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A 5 GHZ BICMOS I/Q VCO WITH 360° VARIABLE PHASE OUTPUTS USING THE VECTOR SUM METHOD

by

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SUMMARY

A 5 GHz BiCMOS I/Q VCO with 360° Variable Phase Outputs using the Vector Sum Method by Tjaart Opperman

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This research looks into the design of an integrated in-phase/quadrature (I/Q) VCO operating at 5 GHz. The goal is to design a phase shifter that is implemented at the LO used for RF up conversion. The target application for the phase shifter is towards phased array antennas operating at 5 GHz. Instead of designing multiple VCOs that each deliver a variety of phases, two identical *LC*-VCOs are coupled together to oscillate at the same frequency and deliver four outputs that are 90 ° out of phase. By varying the amplitudes of the in-phase and quadrature signals independently using VGAs before adding them together, a resultant out-of-phase signal is obtained. A number of independently variable out-of-phase signals can be obtained from these 90 ° out-of-phase signals and this technique is better known as the vector sum method of phase shifting. Control signals to the inputs of the VGAs required to obtain 22.5 ° phase shifts were designed from simulations and are generated using 16-bit DACs.

The design is implemented and manufactured using a 0.35 µm SiGe BiCMOS process and the complete prototype IC occupies an area of 2.65 × 2.65 mm^2. The I/Q VCO with 360 ° variable phase outputs occupies 1.10 × 0.85 mm^2 of chip area and the 16-bit DAC along with its decoding circuitry occupies 0.41 × 0.13 mm^2 of chip area.

The manufactured quadrature VCO was found to oscillate between 4.12 ~ 4.74 GHz and consumes 23.1 mW from a 3.3 V supply without its buffer circuitry. A maximum phase noise of -78.5 dBc / Hz at a 100 kHz offset and -108.17 dBc / Hz at a 1 MHz offset was measured and the minimum VCO figure of merit is 157.8 dBc / Hz. The output voltages of the 16-bit DAC are within 3.5 % of the design specifications. When the phase shifter is controlled by the 16-DAC signals, the maximum measured phase error of the phase shifter is lower than 10 %.

Keywords: Bipolar CMOS (BiCMOS), digital-to-analogue converter (DAC), Gilbert mixer, inductor capacitor (*LC*), integrated circuit (IC), local oscillator (LO), phase noise, phase shifter, phased array antenna, silicon germanium (SiGe), radio frequency (RF), variable gain amplifier (VGA), vector sum method, voltage controlled oscillator (VCO).

SAMEVATTING

'N 5 GHZ BICMOS I/Q VCO MET 360° VERSTELBARE FASE UITSETTE DEUR GEBRUIK TE MAAK VAN DIE VEKTOR SOM METODE DEUR TJAART OPPERMAN

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Hierdie navorsing ondersoek die ontwerp van 'n geïntegreerde in-fase/kwadratuur (I/K) SBO operasioneel teen 5 GHz. Die doel is om 'n faseverskuiwer te ontwerp wat geïmplementeer word by die LO nodig vir RF opverskuiwing. Die teiken toepassing vir die faseverskuiwer is gerig na faserangskikking antennas operasioneel teen 5 GHz. In plaas van om veelvuldige SBOs te ontwerp wat elk 'n verskeidenheid van fases lewer word twee identiese *LC*-SBOs gekoppel om teen die selfde frekwensie te ossilleer en vier fases te lewer wat elk 90 ° uit fase is. Deur die amplitudes van die in-fase en kwadratuur seine onafhanklik te verstel deur gebruik te maak van VWVs voordat hul bymekaar getel word, word 'n resultante uit-fase sein verkry. 'n Verskeidenheid onafhanklike verstelbare uit-fase seine kan verkry word vanaf hierdie 90 ° uit-fase seine en hierdie tegniek is ook beter bekend as vektor som faseverskuiwing. Die beheerseine na die insette van die VWVs wat benodig word om 22.5 ° faseverskuiwings te verkry was ontwerp deur simulasies en word gegenereer deur 16-bit DAOs.

Die ontwerp is geïmplementeer en vervaardig deur gebruik te maak van 'n 0.35 µm SiGe BiCMOS proses en die volledige geïntegreerde stroombaan beslaan 'n area van 2.65 × 2.65 mm^2. The I/K SBO met 360 ° verstelbare fase uitsette beslaan 'n area van 1.10 × 0.85 mm^2 en die 16-bis DAO tesame met die dekoderingstroombaan beslaan 'n area van 0.41 × 0.13 mm^2.

Daar was gevind dat die vervaardigde kwadratuur SBO tussen 4.12 ~ 4.74 GHz ossilleer en 23.1 mW drywing verbruik sonder die buffer stroombane vanaf 'n 3.3 V kragbron. 'n Maksimum faseruis van -78.5 dBc / Hz op 'n 100 kHz afset en -108.17 dBc / Hz op 'n 1 MHz afset was gemeet en die minimum SBO syfer-van-meriet is 157.8 dBc / Hz. Die uitsetspannings van die 16-bis DAO is binne 3.5 % van die ontwerpspesifikasies. Wanneer faseverskuiwer deur die 16-bis DAO beheer word is die maksimum gemete fasefout kleiner as 10 %.

Sleutelwoorde: Bipolêre CMOS (BiCMOS), digital-na-analoog omsetter (DAO), geïntegreerde stroombaan, Gilbert menger, induktor-kapasitor (*LC*), lokale ossilator (LO), faserangskikking antennas, faseruis, faseverskuiwer, radio-frekwensie (RF), silikon-germanium (SiGe), spanningsbeheerde ossilator (SBO), vektor som metode, verstelbare wins versterker (VWV).

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Lastly I would also like to thank my family and friends for their support and motivation.

TABLE OF CONTENTS

LIST OF ABBREVIATIONS

AC	alternating current
BiCMOS	bipolar CMOS
CAD	computer aided design
DAC	digital-to-analogue converter
DC	direct current
DGFET	dual gate field effect transistors
DRC	design rules check
FFT	fast Fourier transform
FOM	figure of merit
GSML	Ground Shield Microstrip Lines
Hit-Kit	high performance interface tool-kit
I/Q	in-phase/quadrature
IF	intermediate frequency
LC	inductor capacitor
LNA	low noise amplifier
LO	local oscillator
LVS	layout versus schematic
MEMS	microelectromechanical systems
MFT	mixed Frequency Time
MOSFET	metal oxide semiconductor field effect transistor
PA	power amplifier
PAC	periodic AC
P-I-N	positive-intrinsic-negative
PNOISE	periodic noise
PCB	printed circuit board
PSP	periodic *S*-parameter
PSS	periodic steady state
PXF	periodic transfer
QPAC	quasi-periodic AC
QPNOISE	quasi-periodic noise
QPSP	quasi-periodic *S*-parameter
QPSS	quasi-periodic steady state
QPXF	quasi-periodic transfer

RF	radio frequency
S-QVCO	series coupled quadrature VCO
SiGe	silicon germanium
SPICE	simulation program with integrated circuit emphasis
TL	transmission line
VCO	voltage controlled oscillator
VGA	variable gain amplifier

1.1 Motivation

Phased array antennas realise the potential of modern wireless communication systems to radiate its energy more efficiently, since a large portion of the radiated energy could be directed towards the receiver. This directional nature of an antenna structure is generally referred to as antenna gain. Apart from the phased array antenna there exist other types of antenna that also achieve directionality, such as a satellite dish. However, the phased array antenna requires no mechanical movement to change its power pattern since this is determined by the amount of phase delay between the different antenna elements. This feature makes phased array antennas suitable for future portable wireless devices, especially now that these devices start operating at much shorter wavelengths, resulting in much smaller antenna structures. That is because the spacing required between adjacent antenna elements is proportional to the signal wavelength. One of the core components required by this type of antenna system is the phase shifter.

A popular method of introducing phase shift is with the aid of transmission lines (TL). By manipulating characteristics of the TL the angle of the phase shift can be controlled. The disadvantage with these types of phase shifters is that the length of line required for 360 ° phase shift is longer than the signal wavelength when travelling at the speed of light. Due to the space limitations of integrated circuits (IC) it becomes unpractical to implement these phase shifters for frequencies below 50 GHz.

For some years now work has been done on phase shifters that obtain phase shifting through the vector sum of orthogonal signals (Chua and Martin, 1998; Guan, Hashemi and Hajimiri, 2004; Gueorguiev, Lindfors and Larsen, 2007; Wu *et al.*, 2006). Because there are no TLs required these phase shifters can be easily integrated onto the same IC as the power amplifier (PA) of most portable wireless devices. This has the benefit of saving cost as well as physical space.

1.2 Justification for the research

Figure 1.1 identifies the scope of this research in relation to the broader research field. This research field stems from work originally done for radar systems (Parker and

Zimmermann, 2002). Phased arrays were later on developed to find its application in the wireless communication systems market (Allen and Ghavami, 2005:xxxv) and these systems are better known as smart or adaptive antennas. This application has motivated the implementation of phase shifters that are more compact (Chua and Martin, 1998; Guan, Hashemi and Hajimiri, 2004; Gueorguiev, Lindfors and Larsen, 2007). This work generally aims towards such applications and focuses on integrating compact low cost phase shifters with other mobile communication circuits on a single IC (Opperman and Sinha, 2008).

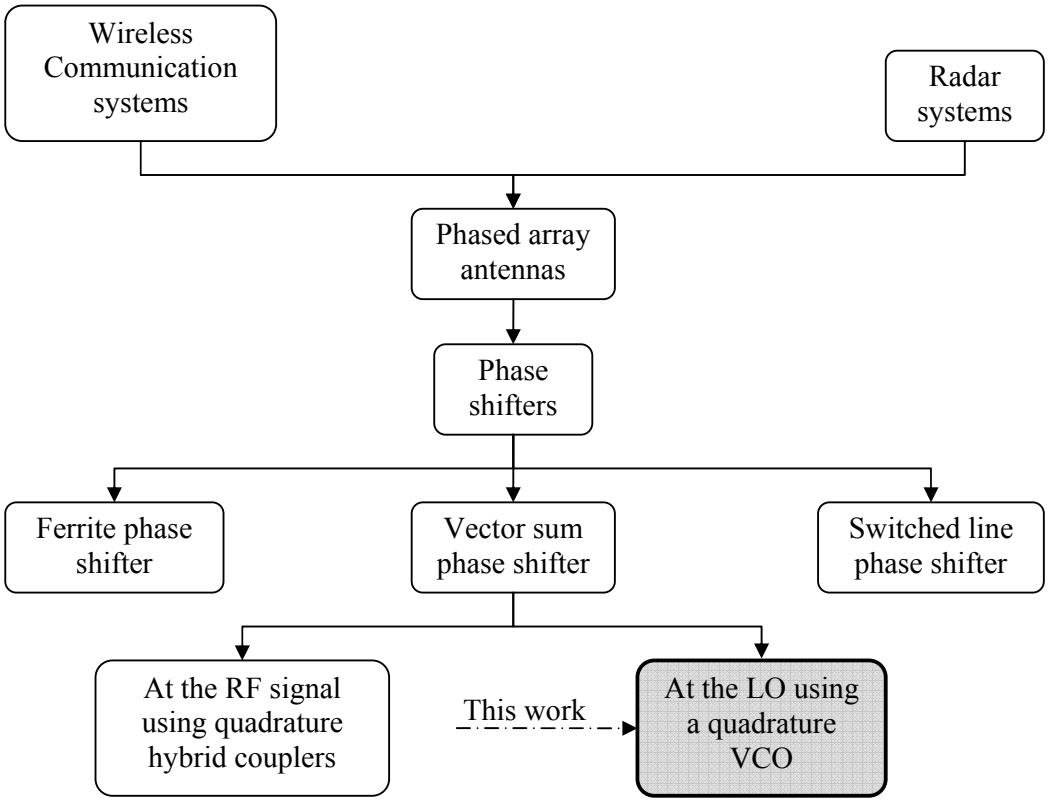


Figure 1.1. Focus of this research problem relative to its broad field of study.

1.3 Research problem

The problem addressed in this research is:

How would the design of an integrated phase shifter, which introduces phase shift using the vector sum method on an integrated quadrature VCO, perform at 5 GHz when the phase shift is to be applied at the LO?

It is expected that the integrated design will enable a phase shifter to be smaller and cheaper when compared to other methods of phase shifting. The power handling capabilities of the phase shifter will also be lower than that of conventional phase shifters and is therefore integrated to form part of the LO.

Performance indicators include:

- device power consumption,
- manufacturing cost,
- device size,
- phase noise, and
- phase error.

Power handling capability should also be used as an indicator but since the design forms part of a LO, it is assumed that a low power baseband signal or an incoming radio frequency (RF) signal is applied as an input to the design and that an integrated active circuit is then used to add the required power after the phase shift has been introduced at the LO.

1.4 Organisation of dissertation

The following outlines the organization of this dissertation.

- Chapter 2: Literature review

The chapter reviews previous work that lead to the development of this subject and evaluates their contributions and results so that this work may be placed into context. It also highlights some of the underlying theories related to this subject.

- Chapter 3: Design methodology

The chapter describes the design methodology used to develop the proposed design into a functional circuit as well as the measurement setup used to experimentally validate the design.

- Chapter 4: Circuit design

The chapter presents the design, simulation and layout of the prototype circuit. The active and passive devices are first characterised and then these results are used for the circuit design. The circuit floor plan and printed circuit board (PCB) design are then presented.

- Chapter 5: Full circuit simulation and measurement results

The chapter presents the measurement results of the prototyped IC and compares it to that of circuit simulations. Conclusions about these results are drawn and deviations from expected simulation results are explained.

- Chapter 6: Conclusion

The chapter summarises this research and its results and draws concluding remarks about the work. Recommendations for future work are also presented in line with the shortcomings of this work.

The dissertation also includes two appendices. The first appendix presents the behavioural description of the digital circuit as well as its circuit schematic. The second appendix presents the layouts of some of the core circuit components as well as photographs taken from the prototyped design of these components.

1.5 Delimitations of scope and key assumptions

The circuit design for this research is implemented using a 0.35 µm SiGe BiCMOS technology. In industry the choice of technology is usually based around cost and performance. This work is not aimed towards a specific implementation but presents a broad application aimed at wireless communication systems and radar systems in general. Depending on the type of application a selection should be made on the technology to use. From the list of technologies available from the current manufacturer this specific technology is ahead in terms of high frequency performance (Austriamicrosystems AG, 2008) but is amongst the most expensive of choices. If for instance the application is aimed at a low cost solution but compromised high frequency performance specifications, a CMOS only implementation could be applicable.

2.1 Introduction

Section 1.1 presented a motivation for this research and section 1.2 identified the context of this work in relation to previous work. This chapter reviews previous publications, identify past achievements as well shortcomings in this field. The basic theory behind phase shifters and quadrature voltage controlled oscillators (VCO) is also reviewed.

2.2 Phase shifters

A popular method of introducing phase shift is with the aid of TLs. The propagation delay of TLs results in a change in phase of the signal passing through it. In general, for a lossless or a distortionless line, the phase velocity is (Cheng, 1993:349)

$$u_p = \frac{1}{\sqrt{\mu\varepsilon}} = \frac{c}{\sqrt{\mu_r \varepsilon_r}}, \tag{2.1}$$

where μ and μ_r are the permeability and relative permeability of the metal, ε and ε_r are the permittivity and relative permittivity of the dielectric and c is the speed of light in a vacuum. For a given lossless or distortionless TL, the length of TL required for 1 ° of phase shift is therefore

$$l_{1^\circ} = \frac{c}{360^\circ f_0 \sqrt{\mu_r \varepsilon_r}}, \tag{2.2}$$

where f_0 is the frequency of the signal.

Positive-intrinsic-negative (P-I-N) diodes can be used to design phase shifters. The ON/OFF state of the diode is controlled by changing the direct current (DC) bias voltage across it (Pozar, 2005:518). By connecting a number of TLs of different lengths using P-I-N diodes a phase shift can obtained as described in equation (2.2). This type of phase shifter is known as a *switched line* phase shifter. Microelectromechanical systems (MEMS) phase shifters operate on the same principle using electromechanical switching instead but have relatively low power handling capabilities (Parker and Zimmermann, 2002).

Another type of well known phase shifter is a ferrite phase shifter. There are four general types of phase shifters namely variable permeability, nonreciprocal toroidal, dual mode and rotary field phase shifters (Parker and Zimmermann, 2002). The nonreciprocal toroidal

phase shifter was considered by Pozar (2005:471) to be one of the most useful designs. This phase shifter consists of a toroidal ferrite core located inside a waveguide with a bias wire passing through its centre. A variation in the phase shift results from the dependence of its magnetic properties on the current flowing through the bias wire.

Vector sum phase shifting is achieved by adding two or more out-of-phase signals (usually by a quarter of a cycle) together as illustrated in Figure 2.1. As the amplitudes of both signals are varied independently, the resulting phase will vary accordingly and for quadrature signals the resulting phase is given by

$$\varphi = \tan^{-1}\left(V_Q / V_I\right), \tag{2.3}$$

where V_I and V_Q denotes the amplitudes of the in-phase and quadrature signals respectively. The resulting amplitude is given by

$$V_{res} = \sqrt{V_Q^2 + V_I^2}\ . \tag{2.4}$$

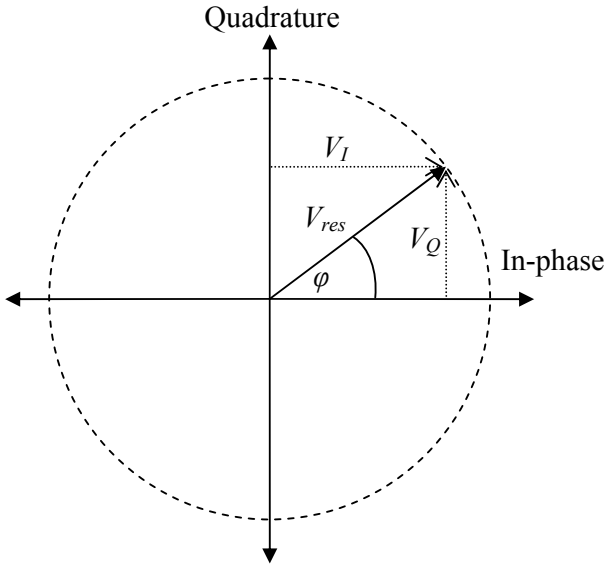


Figure 2.1. A phasor representation of the vector sum method.

(Kim and Myung, 2000) proposed an active phase shifter using the vector sum method. An incoming RF signal is split into two out-of-phase signals using two variable gain amplifiers (VGA), a 3 dB quadrature hybrid coupler and a 180 ° phase shifter. These two resulting signals are not necessarily out-of-phase by 90 °. Two more VGAs are then used along with an in-phase power combiner to produce the vector sum of the two out-of-phase signals. The VGAs are implemented using dual gate field effect transistors (DGFET). The

proposed active phase shifter was designed and implemented in the $2.2 \sim 2.3$ GHz frequency range, on microstrip using packaged DGFETs for the VGAs. A similar approach was used by Wu, Chang, Tsai, Huang and Wang (2006) to design two similar but different phase shifters operating in the $15 \sim 20$ GHz frequency range using the vector sum method. The presented designs are implemented using TSMC's 0.18 µm MS/RF CMOS technology instead (Taiwan Semiconductor Manufacturing Company Limited, 2008). The individual chip sizes for both designs are $0.95 \times 0.76\ \text{mm}^2$ and $0.71 \times 0.82\ \text{mm}^2$. This work demonstrated the first CMOS based microwave phase shifter using the vector sum method as well as the smallest chip size for its type in this frequency range. Chua and Martin (1998) presented a single chip implementation of a phase shifter using 0.8 µm silicon bipolar technology. The incoming RF signal is split into two differential equal amplitude quadrature signals using a RC polyphase network. Vector sum phase shifting is then implemented using these quadrature signals. A 6-bit digital-to-analogue (DAC) is used to control the VGAs.

In general phase shifting is applied directly on the incoming or outgoing RF signal. Guan, Hashemi and Hajimiri (2004) presented the design and measurement of a fully integrated phased array receiver that achieves phase shift at the local oscillator (LO). A discrete number of phases are obtained using a ring inductor capacitor (*LC*) VCO that consists of eight differential CMOS amplifiers with tuned *LC* loads connected in a ring (Guan, Hashemi, Komijani and Hajimiri, 2004). For every antenna element a phase selector is used to select one of the 16 VCO phase outputs to be used to down convert the RF signal. The phase shift present in the LO propagates through the demodulator onto the down converted signal. A similar approach could also be taken at the transmitter side as well, whereby the phase shift is applied to the LO being used for RF up conversion. The concept is illustrated in Figure 2.2 and a circuit design based on this is presented by Gueorguiev, Lindfors and Larsen (2007). The reported phase shifter operates using an external VCO at 5.2 GHz and the measured phase accuracy is better than 5 ° over the entire phase shift range. The quadrature LO signals are obtained using a frequency divider and then phase shifted using the vector sum method. The LO signals are then modulated with itself to up convert it again. Colom, Castañeda and Knapp (2008) presented the design and measurement of a phase shifter for X-band phased array applications using the vector sum method at the LO of the intermediate frequency (IF) mixer. A single chip solution was however not presented. Parker and Zimmerman (2002) summarized the typical

performance parameters of various phase shifters and it was reported that the rotary field ferrite phase shifter has by far the highest power handling capability but is the bulkiest and quite expensive when compared to other phase shifters. The integrated phase shifter provides a low cost, small size alternative at the expense of power handling capability.

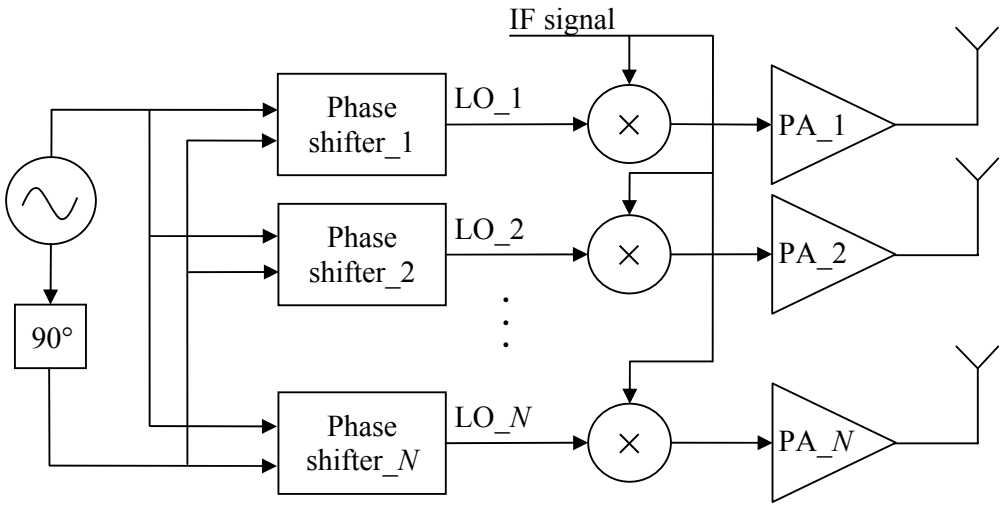


Figure 2.2. Illustration of how the phase shift propagates from the LO to the PA when it is modulated with the IF signal.

2.3 Quadrature oscillators

As mentioned in section 2.2 the vector sum method requires two or more out-of-phase signals to produce a resulting phase shift. In this work, the phase shift is introduced at the LO as illustrated in Figure 2.2 and the design of a quadrature oscillator is looked at. The vector sum method is therefore based on the summing of two quadrature signals by varying their amplitudes.

One of the main design specifications of a VCO is its phase noise performance. In general the output signal of a VCO is given by

$$v_{OSC}(t) = V_O(t)\cos\left[2\pi f_c t + \varphi(t)\right], \tag{2.5}$$

where f_c is the centre frequency of the oscillator. Because of the time varying nature of both the amplitude, $V_O(t)$ and phase, $\varphi(t)$ of the centre frequency, sidebands around this centre frequency are created (Tiebout, 2005:5). The relationship of the power spectral

density $P_{sideband}$ in these sidebands at a certain offset frequency Δf, relative to the power of the carrier $P_{carrier}$ is known as the phase noise and given by

$$L(f_c, \Delta f) = 10\log_{10}\left[\frac{P_{sideband}(f_c + \Delta f)}{P_{carrier}}\right], \tag{2.6}$$

which is measured in dBc / Hz.

Another important design specification of a VCO is its power consumption. It is useful to analyse the performance of a VCO with respect to its phase noise performance as well as its power consumption. The VCO figure of merit (FOM) indicates this performance and is given by (Casha, Grech and Micallef, 2007)

$$\text{FOM} = -L(f_c, \Delta f) + 10\log_{10}\left(\left(\frac{f_c}{\Delta f}\right)^2 \frac{1\,\text{mW}}{P_{supply}}\right), \tag{2.7}$$

where P_{supply} is the power consumption of the VCO. The FOM is also measured in dBc / Hz and a higher value of FOM indicates a better performing VCO.

Two main types of oscillators are known as the harmonic oscillator and the relaxation oscillator. A harmonic oscillator produces a sinusoidal output and consists of an amplifier circuit and a filter. The harmonic oscillator can be analysed as a gain stage with a feedback circuit as shown in Figure 2.3. The overall gain for this circuit is given by

$$G = \frac{v_{out}}{v_{in}} = \frac{A(j\omega)}{1 + A(j\omega)H(j\omega)}, \tag{2.8}$$

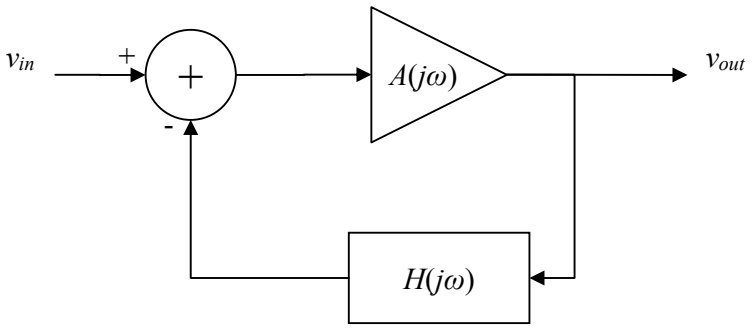


Figure 2.3. Block diagram of a feedback circuit.

where $A(j\omega)$ is the open loop gain and $H(j\omega)$ the transfer function of the feedback circuit. When there is no signal applied at the input of this loop there will be no output. If

$|A(j\omega)H(j\omega)| > 1$ at the frequency where $\angle A(j\omega)H(j\omega) = -180°$ the loop will be unstable and oscillate (Gray, 2001:628).

Another analysis on the harmonic oscillator is based on the concept of negative resistance. This theory is mostly applied to analyse harmonic oscillators with an inductor and capacitor in parallel (Sinha, 2005:79). The impulse response of an *LC*-tank circuit results in a sinusoidal voltage across the tank. When there is a resistive element in parallel with the *LC*-tank, the voltage will decay with time because energy is being dissipated in the resistor. Figure 2.4 shows an *LC*-tank circuit with a parasitic resistive element R_P in parallel with the tank. For an ideal *LC*-tank circuit R_p would be infinite but due to the parasitic series resistance of the both the inductor and capacitor, R_p has a finite value. If a resistance of $-R$ is also placed in parallel with the tank and $R = R_p$, the combined resistance would be infinite. The negative resistance is obtained using one or more active components such as diodes or transistor configurations that exhibit negative resistance (Pozar, 2005:521) and for practical reasons usually $R > R_p$.

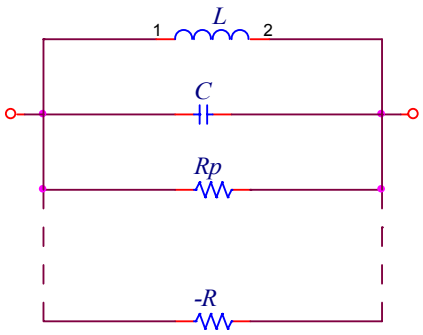


Figure 2.4. An *LC*-tank circuit with a parasitic resistive element in parallel with a negative resistance.

Both analysis methods assume that the tank circuit already has a sustained oscillation. The feedback circuit in Figure 2.3 would not oscillate if $v_{in} = 0$ V and the negative resistance circuit oscillator would also not oscillate even when $R_p > R$ and there is no initial harmonic signal. However, noise generated by the active devices propagates into the feedback circuit of Figure 2.3 and the tank circuit of Figure 2.4. In theory this noise would cause oscillations to grow indefinitely. In practice however both the open loop gain $A(j\omega)$ as well $-R$ depend on the large signal oscillation voltage V_{osc}. As V_{osc} increases over time from the noise generated by the active circuit, $-R$ increases until $R_p = -R$. Afterwards any increase in

V_{osc} resulting from noise is dissipated in the tank circuit since $R_p < R$, and this in return decreases V_{osc} again. Therefore in order to find settling value for V_{osc}, one has to solve

$$R_p - R(V_{osc}) = 0 \tag{2.9}$$

The relaxation oscillator operates by charging a capacitor up to a certain upper threshold voltage before discharging it rapidly. When the capacitor is discharged below a certain lower threshold voltage the capacitor is charged up again. The switching is implemented using an active device such as a diode or comparators. When integrated, these oscillators have very small area and are easy to design (Tiebout, 2005:10). However, due to the low FOM of relaxation oscillators when compared to harmonic oscillators (Eken and Uyemura, 2004; Park and Kim, 1999) these will not be considered as part of this research.

For this dissertation the implementation of a 5 GHz VCO is considered. As discussed in section 2.2 the phase shifter implementation requires the VCO to have quadrature outputs. Since a bipolar CMOS (BiCMOS) process is used, literature on both CMOS and BiCMOS oscillators are reviewed. Casha, Grech and Micalief (2007) presents a comparative study of CMOS quadrature *LC*-VCOs with relevance to phase noise. In this study the authors identify six main methods of achieving quadrature outputs by coupling two differential *LC*-VCOs. From this comparative study a quadrature *LC*-VCO from Yao and Willson (2006) operating at 5.1 GHz was identified as having the highest FOM of 193 dBc / Hz at the time. The VCOs are coupled together using two separate *LC*-tanks which results in a total circuit layout area as large as 1.9×1.8 mm^2. In general all the research based on inductive coupling result in relatively large circuit areas, due to the relatively large size of on-chip inductors. However, the transformer based coupling method presented by Ravi, Soumyanath, Carley and Bishop (2003) uses a 6-metal 0.18 µm low voltage digital CMOS process to realise a 5 GHz quadrature VCO with a FOM of 177 dBc / Hz and a circuit area[1] of 0.26 mm^2 with a power dissipation of 12 mW. Even though this work presents a quadrature VCO with a relatively high FOM and a small circuit area, it requires the availability of a 6-metal process. Cho, Tsai, Chang and Wang (2006) present a series coupled quadrature VCO (S-QVCO) operating a 5.7 GHz using a similar process that achieves a FOM of 183 dBc / Hz with a circuit area of 1×0.65 mm^2 and a power

[1] The reference actually reports an oscillator core area of 0.26 µm^2, but from intuition it is suspected that this might be a typing error and the authors probably meant 0.26 mm^2.

dissipation of 14.4 mW. Based on the FOM it can be concluded that both designs perform similarly with the latter consuming double the amount of chip area considering that both circuits are implemented using similar processes.

Kim, Cha, Oh, Yang and Lee (2004) propose a novel circuit that uses the back-gates of the $-g_m$ transistors to couple two *LC*-VCOs together in order to obtain quadrature outputs. The proposed circuit operates form 1.047 ~ 1.39 GHz and achieves a FOM of 174 dBc / Hz. The main disadvantage of this implementation is that it requires a triple well process. Chung and Cheng (2007) propose a quadrature *LC*-VCO circuit that uses the back-gates of the PMOS current sources to couple the second harmonic signal of two identical *LC*-VCOs. The main advantage is that this technique does not require a triple well process in order to implement back-gate coupling. The proposed circuit was manufactured using a 0.35 µm standard CMOS process with four metal layers and achieves a FOM of 179 dBc / Hz. The oscillation frequency is from 4.47 ~ 5.08 GHz with a chip area of 0.5×1.6 mm^2.

A VCO operating from 4.2 ~ 5.4 GHz using a 0.35 µm SiGe BiCMOS technology is presented by Esame, Tekin, Bozkurt and Gurbuz (2007). This work utilises a similar technology to that proposed for this work. Measurement results on the actual circuit are not presented but post-layout simulation results are given. The simulated VCO achieves a FOM of 178 dBc / Hz with a chip area of 0.6 mm^2. Considering an ideal case where the coupling circuitry does not consume any power an equivalent quadrature VCO would obtain a FOM that is 3 dB lower than the single VCO. Kakani, Dai and Jaeger (2007) present an S-QVCO using a similar technology that utilises HBTs for oscillation and metal oxide semiconductor field effect transistors (MOSFET) for coupling. The presented quadrature VCO operates from 4.3 ~ 5 GHz. It is suggested that the NPN transistors achieve a high oscillation frequency while the MOSFETs provide more headroom, better isolation and an increased tuning range. The S-QVCO coupling technique also reduces the power consumption of the circuit but results in a reduction in voltage headroom for the output swing. The presented quadrature VCO achieves a FOM of 169 dBc / Hz with a chip area 0.88 mm^2. Given the superior high frequency performance capabilities of the HBTs for the proposed process technology as discussed in section 1.5 as well as the relatively high FOM for the latter quadrature VCO, an implementation of this quadrature VCO will be further investigated.

2.4 Conclusion

A review on phase shifters was presented and a literature review was done which focussed toward the vector sum method implemented at the LO. A review was also done on quadrature oscillators and a literature review was done which focussed on 5 GHz quadrature VCOs. This dissertation will now continue by presenting the design methodology used to develop this theory into a functional circuit.

CHAPTER 3: DESIGN METHODOLOGY

3.1 Introduction

Chapter 2 combined the theories that describe the operation of the proposed circuit. It also evaluated recently published circuit designs relevant to this research. Chapter 3 describes the design methodology used to transform this theory into a functional circuit that can be physically measured. An introduction to this chapter was provided in section 1.4 of chapter 1 and this chapter aims to build on that. This chapter is organized around four major topics: design methodology outline, IC manufacturing, CAD tools and measurement setup and afterwards concluding remarks are presented.

3.2 Design methodology outline

As part of this research, an actual IC was designed and measured. The physical measurement of the entire design after its fabrication supports the theory that describes its operation as well as the feasibility of its application. As an intermediate step towards fabrication, the design was simulated and verified using CAD tools. These tools play an important role in the design process as well. Firstly, it characterizes the circuit model with more precision than can be accomplished when using hand calculations. This enables the circuit to be optimized in order to achieve the desired design specifications. Secondly, these tools can spot fatal design flaws such as unreliable current densities or inconsistencies between the circuit schematic and the physical layout. The first step of any subsystem design was commenced by using hand calculations on simplified circuit models in order to solve the circuit component values. This initial step enabled the circuit to be evaluated critically in order to make intelligent choices about component values, which established a rough starting point for CAD optimization. During the entire design process the chosen circuit topology for every subsystem was also evaluated critically. This evaluation was based on the subsystem's performance when compared with similar designs from literature as well as its compatibility with the neighbouring stages. An outline of the design methodology applied to the subsystem design is presented in Figure 3.1.

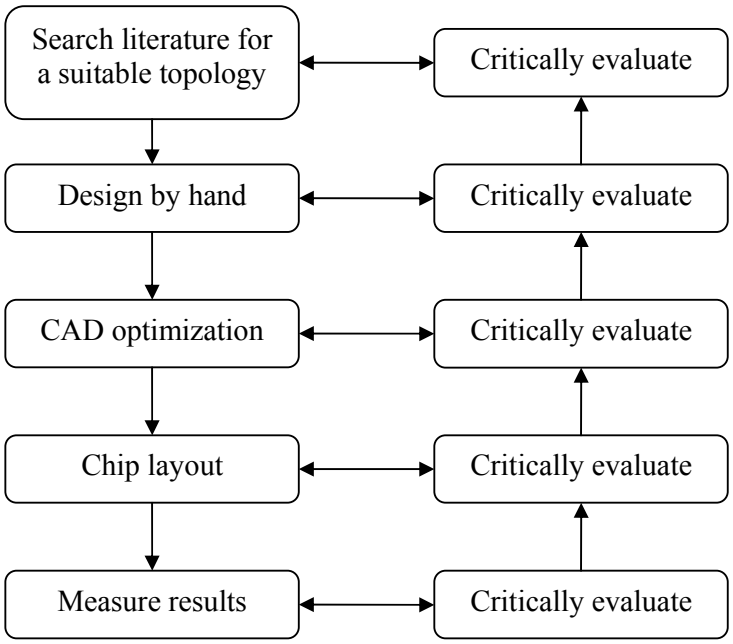


Figure 3.1. An outline of the design methodology applied to each subsystem.

3.3 IC manufacturing

The manufacturing of the IC was done using the *S35 0.35 µm SiGe BiCMOS process* from Austriamicrosystems. The main features of this particular IC process are (Austriamicrosystems AG, 2008):

- SiGe BiCMOS process with NPN HBTs,
- four layers of poly-silicon including a high-resistive poly layer,
- four layers of metal including a thick metal layer,
- feature sizes: 0.35 µm gates and 0.4 µm emitters,
- f_t > 60 GHz and f_{max} > 70 GHz,
- BV_{CEo} > 2 V,
- CMOS supply voltage: 3.3 V,
- PIP and MIM capacitors, and
- core 3.3 V CMOS digital cell libraries.

The overall circuit performance is to a large extent determined by the specific IC process being used. The characteristics of this IC process have been measured up to 6 GHz by the

foundry for most of the components that are provided (Austriamicrosystems AG, 2005b). The lateral and vertical PNP transistors are not characterized at RF and the foundry provides simulation models for these transistors that are only valid up to 800 MHz (Austriamicrosystems AG, 2005a). The foundry does not recommend the use of the diode models therefore diode connected HBTs were used instead.

A list of on-chip spiral inductors ranging from $1 \sim 20$ nH have been designed and characterized up to RF by the foundry and are made available to the circuit designer (Austriamicrosystems AG, 2005b). This assists with the circuit design in the following manner. Firstly, given the relatively large size of inductors, the list of inductors gives the circuit designer the flexibility to select inductors that enables the entire circuit to fit onto the desired chip area. This selection could already be made at an early stage of the design because the dimensions of the inductors would be known beforehand. If it should become apparent that the inductors take up too much space, the circuit can be redesigned to use less or smaller inductors. This prevents one from wasting valuable time designing a circuit that will eventually not fit or, unnecessarily consume more space which cannot be justified by the performance gained when utilizing more or bigger inductors. Secondly, using inductors that have been fully characterized at the desired operating frequency makes the behaviour of the final design more predictable. Lastly, it saves time when the main focus of the dissertation is not directed towards the design of on-chip spiral inductors.

When the targeted application has many consumers, the main performance indicator of any IC process should be based on its cost per chip. SiGe BiCMOS processes are usually more expensive per chip than CMOS only processes. The justification for the use of this more expensive technology was already mentioned in section 1.5. The use of this particular SiGe BiCMOS process should however still be justified. The cost of prototyping is much higher than the cost of the manufacturing of large quantities would be. IC foundries usually only give quotations for large scale manufacturing after the design have been submitted. It would not be economically viable to design a prototype circuit for every compatible IC process in order to obtain the lowest bid. An IC process would therefore have to be selected based on the foundry's long-standing competitive reputation and also based on the suitability of its available technologies toward the specifications of the circuit. One would not expect to pay more for an inferior IC process, given that both foundries are well known for being competitive. For example, if there are two IC processes available from two

different but eminent foundries, it would make sense to use the IC process that meets the requirements of the circuit specifications rather than using the one that overachieve these requirements. Based on these criteria, the abovementioned IC process was chosen for this dissertation.

3.4 Computer aided design (CAD) tools

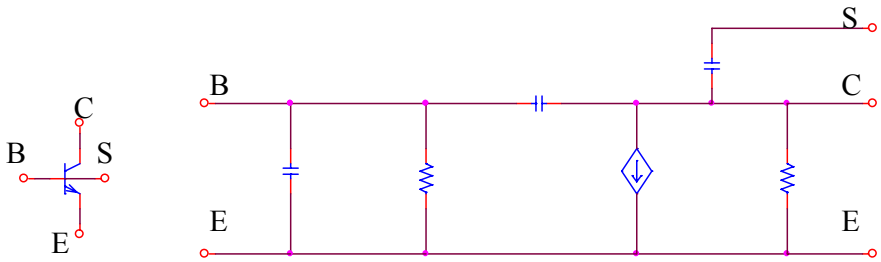
The role of CAD tools as part of this research has been introduced in the design methodology outline of this chapter. A short background on the functional behaviour of some of these tools will be discussed to explain how it will be used to assist during the design process.

3.4.1 Simulation program with integrated circuit emphasis (SPICE)

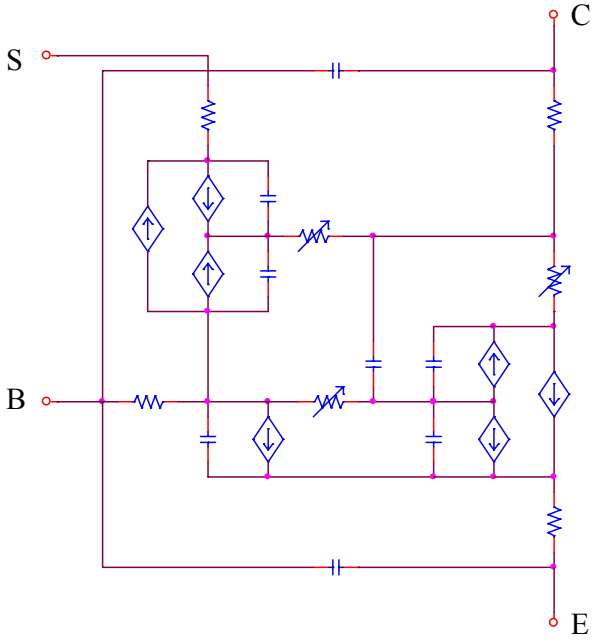
SPICE is a program that can be used to predict the behaviour of a circuit. The circuit that is to be simulated is contained in a netlist. The netlist is a text file that describes how the ports of every primitive component contained in the circuit are connected together. The program then solves the currents and voltages for the entire circuit as a function of time. SPICE can also find the DC solution of the circuit. It does this by setting the values of all time-varying sources to zero, removing capacitors from the circuit and replacing inductors with wires. The DC solution can also be used as a starting point for alternating current (AC) analysis. For the AC analysis, all of the non-linear elements are linearised around the DC operating and then replaced by linear elements. The inductive and capacitive elements are reintroduced and the magnitudes and phases of the currents and voltages are then solved for the specified frequencies (Tanner EDA, 2007).

Non-linear elements such as transistors, diodes and resistors, are supported by SPICE through primitive models. There are a variety of different SPICE primitive models available and these may vary between different vendors. The model describes the general behaviour of an element. The model parameters describe the specific behaviour of a device and are obtained from physical measurements that have been done on the device. The instance parameters refer to the specific geometric details of a device being instanced and this will scale the model parameters accordingly. To illustrate the capacity of SPICE, the

typical equivalent circuit of a bipolar transistor used for doing hand calculations and that used by SPICE are shown in Figure 3.2a) and b) respectively.



a)



b)

Figure 3.2. A typical equivalent network of a bipolar transistor used for a) hand calculations and b) for SPICE simulations.

The bipolar model presented in Figure 3.2a) is based on the Gummel-Poon model (Gummel and Poon, 1970). The bipolar model in Figure 3.2b) is an extract of the VBIC95 model[2]. This model includes parasitic effects that are important for the accurate modelling

[2] More information on the VBIC model can be obtained by visiting http://www.designers-guide.org/VBIC/index.html.

of bipolar transistors and is also reported to have improved S-parameter fits (McAndrew *et al.*, 1996). The IC foundry provides SPICE models which are valid up to 6 GHz for most of its components.

3.4.2 RF simulations

Apart from SPICE, some developers have made tools available that will assist with RF circuit design. Examples of these are SpectreRF (Cadence Design Systems, 2005b) and EldoRF (Mentor Graphics, 2006). In particular, these tools aid with the design of VCOs, VGAs, low noise amplifiers (LNA) and PAs. Frequency translation which occurs when large signals are applied to non-linear devices is effectively simulated by these tools. A summary of some of the important features of these tools provided by SpectreRF is presented below. The scope of this summary is focused towards the tools that were regarded as being useful to this research.

3.4.2.1 Periodic steady state (PSS) analysis and quasi-periodic steady state (QPSS) analysis

This is the first phase of the RF simulation. The PSS analysis computes the periodic operating point of the circuit which is required for periodic small signal analyses. By using a method known as the *shooting method,* the initial condition that results in the circuit being periodic is found (Cadence Design Systems, 2005a). The simulation time is independent of the circuit time constant.

PSS supports circuits which are autonomous and non-autonomous. Autonomous circuits are defined as time-invariant circuits with time-variant responses. An example of an autonomous circuit is an oscillator. Non-autonomous circuits include mixers and amplifiers. When an autonomous circuit is to be simulated, an estimation of the oscillation period must be provided. The PSS analysis for an autonomous circuit is preceded by a transient analysis so that the circuit may first be initialized.

QPSS analysis enables the circuit response to be computed for several large input signals in addition to a strongly non-linear tone representing a LO. Fundamentals that are closely

spaced or disproportionate cannot be effectively resolved by the PSS analysis and the QPSS analysis must be used instead. The QPSS uses the Mixed Frequency Time (MFT) algorithm extended to multiple fundamental frequencies (Kundert, White and Sangiovanni-Vincentelli, 1990).

3.4.2.2 Periodic small-signal analyses and quasi-periodic small-signal analyses

The periodic small-signal analyses include the periodic AC (PAC) analysis, the periodic *S*-parameter (PSP) analysis, the periodic transfer (PXF) analysis and the periodic noise (PNOISE) analysis. The PSS analysis must always precede the periodic small-signal analyses. The periodic small-signal analyses are applied to circuits that exhibit frequency translation. The conventional small signal analysis provided by SPICE in general does not support this feature. This stems from the fact that the circuit is linearised around its DC operating point when using SPICE in general. When using PSS, the circuit is linearised around its periodically time-varying operating point obtained when large signals are applied to it. A periodically time-varying circuit exhibits frequency translation. This operating point can be used by the periodic small-signal analysis to predict the response of the circuit when additional small signals are applied to it at arbitrary frequencies.

The quasi-periodic small-signal analyses include the quasi-periodic AC (QPAC) analysis, the quasi-periodic *S*-parameter (QPSP) analysis, the quasi-periodic transfer (QPXF) analysis and the quasi-periodic noise (QPNOISE) analysis. The QPSS analysis must always precede the quasi-periodic small-signal analyses. The quasi-periodic small-signal analysis differs from the periodic small signal analysis in that it computes the frequency translation for multiple large-input signals as well as the intermodulation distortion caused by these multiple large signals when applied to non-linear circuits. With the periodic small-signal analysis, there can only be one large signal and the intermodulation distortion contributed by the other signals is calculated with the assumption that these were all small signals. Therefore, a quasi-periodic small-signal analysis with one large signal and multiple small signals would produce similar results as a periodic small-signal analysis when the same signals are applied to it. The periodic small-signal analysis would however be faster to simulate. The periodic small-signal analysis on the other hand would not

provide accurate results when more than one of the signals have large amplitudes and the circuit response is non-linear.

3.4.2.3 Oscillator noise analysis

Phase noise occurring in oscillators can be simulated using SpectreRF. Phase noise is one of the primary specifications of an oscillator and is its most significant source of noise. Because the phase noise is located very close to the carrier it cannot be easily filtered out with the low *Q* on-chip inductors available (Tiebout, 2005:21). The phase noise stems from a variety of sources in the oscillator design and an assortment of design approaches have been investigated that could lower phase noise (Casha, Grech and Micallef, 2007; Hajimiri and Lee, 1999; Kim and Kim, 2000; Zhan *et al.*, 2003). Even though these design approaches were implemented using specific IC processes as part of experimental proof, these techniques can be generalized provided that the IC process to be used does have similar characteristics. It is however important to optimize the oscillator design for the IC process that will be used in this dissertation, in order to improve the phase noise performance. Oscillator noise analysis using SpectreRF introduces a cost effective way to accurately verify that the design has been optimized to achieve sufficient phase noise performance before manufacturing commences.

3.4.3 Circuit layout

The last step of the IC design involves the layout of the physical circuit. Even though the layout of digital circuitry is mostly computer automated (as will be discussed in the following section), the layout of analogue circuitry was done by hand. When laying out large analogue circuits by hand, the probability of introducing human error is augmented. Fortunately there are CAD tools available that will allow the designer to compare the physical circuit layout with its corresponding schematic. This tool is generally referred to as layout versus schematic (LVS).

Apart from the parasitic elements present in circuit components which have been measured by the foundry, circuit wires that connect components together also introduce parasitic elements and can cause unwanted signal coupling between wires. The impact of this effect

becomes more significant as the frequency of interest increases. Fortunately there are also CAD tools available that will analyze the circuit layout and extract these parasitic elements. The effect of these additional unwanted parasitic elements can then be simulated and investigated.

In order to ensure that the circuit layout is compatible with the IC manufacturing process, the foundry usually provides a set of design rules that must be rigorously followed. These rules also guide to designer to design ICs that will contain less defects when implemented on the relevant IC process (Austriamicrosystems AG, 2004). There are also CAD tools available that will evaluate the physical circuit layout and report any design rule violation. This tool is generally referred to as design rules check (DRC).

3.4.4 Digital design

Digital design is often automated from a behavioural description right down to the circuit layout. The functional behaviour of the circuit is introduced using the VHDL programming language (Ashenden, 2008). A VHDL synthesizer transforms the behavioural circuit description into a digital circuit that only consists of core library components available from the specified IC process. For this dissertation the Precision RTL Synthesis from Mentor Graphics® will be used together with the 3.3 V standard cell core libraries from Austriamicrosystems. The VHDL synthesizer uses a technology file that contains the timing information and area utilization of all the available digital cells from the specified IC process's core library. The synthesizer will compile the VHDL code to optimize for either area or speed. After compilation, the complete digital circuit is contained in a netlist.

After a netlist has been created, the next step is to physically lay the circuit out. An automatic place and route application can be used for this. The ICblocks design environment provided by Mentor Graphics® will be used for this. This application uses the standard digital cells which have already been laid out by the IC foundry, together with the circuit netlist in order to automatically place and route the complete layout. An outline of the design methodology applied to digital design is shown in Figure 3.3.

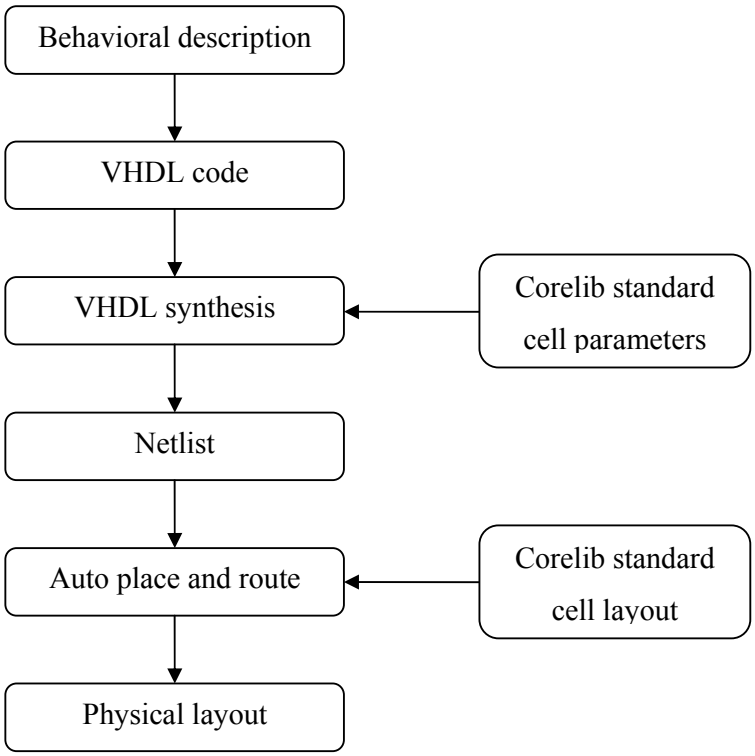


Figure 3.3. An outline of the design methodology applied to digital design.

3.4.5 The high performance interface tool-kit (Hit-Kit)

The utility of the CAD tools available for mixed signal IC design has already been discussed. These tools analyze the design based on the characteristics of the relevant IC process. The Hit-Kit is a collection of software programs and libraries that contain the all the information required by the abovementioned tools for the design of digital as well as analogue circuits[3]. This information includes SPICE models, design rules and standard cell libraries. The Hit-Kit is supplied by the IC foundry and usually only supports a limited number of CAD platforms.

[3] More information on the Austriamicrosystems Hit-Kit can be obtained from http://asic.austriamicrosystems.com/hitkit/general/hitkit.html.

3.5 Measurement setup

The integrity of the experimental data relies on the accuracy measurement setup. The primary concern here is the equipment being used. Accurate measurement required the use of high quality measurement tools that were calibrated. For RF phase measurements the *Agilent E5071B RF Network Analyzer* was used. It was the responsibility of a certified third party laboratory to ensure that the equipment were available and were also calibrated. The RF phase measurement setup is shown in Figure 3.4.

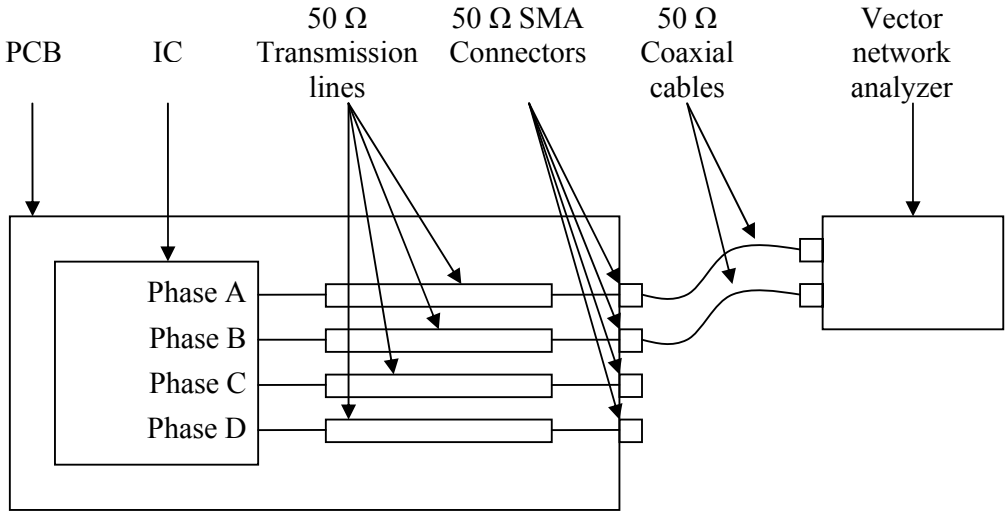


Figure 3.4. RF measurement setup.

Since the frequency of interest is at RF, another important aspect that requires attention will be the evaluation PCB design. The characteristic impedance of the entire design, which includes connectors, TLs and cables, should be 50 Ω. This value was chosen in order to comply with the characteristics of coaxial cables and is also widely used by the RF measurement equipment. Therefore to ensure maximum power transfer, the output impedance of the analogue IC design should match 50 Ω. In general, TLs must be used for circuit design when the electrical length is more than 1/20 of the wavelength (Schmitt, 2002:8). Since the frequency of interest is mostly around 5 GHz and assuming that the permittivity of PCBs is mostly around 4.5, wire lengths of more than 1.4 mm should be treated as TLs. For this dissertation 3 types of PCB TLs were considered namely: microstrip lines, coplanar waveguides with a ground and striplines. Figure 3.5 shows a cross-section of these 3 types of TLs (Wadell, 1991).

To ensure that the PCB TLs were of a high quality, the lines:

- had to have a 50 Ω characteristic impedance,
- had to have equal length,
- had to extend to the edge of the PCB,
- were to have a minimum number of bends,
- had to have minimum number of vias, and
- had to be routed first.

Usually the permittivity of the board (ε_r), the spacing between layers (h) and the thickness of the metal layers (t) are fixed and determined by the PCB fabrication process. The width of the lines (w, a) and the spacing of the adjacent ground planes (b) were parameters that needed to be determined in order to design for a 50 Ω characteristic impedance. Figure 3.6 shows a plot of these ratios required for a 50 Ω characteristic impedance coplanar waveguide with ground TL (Wadell, 1991:79). For this type of TL, the convenience lies in the fact that the line width (a) can be chosen to be the same as either the IC package pin width or the pin width of the PCB coaxial cable connector[4]. The adjacent ground plane spacing (b) can then be read off from the graph. It is recommended that $h >> b$ and that the top layer ground planes are much wider than b (Riaziat *et al.*, 1987).

[4] A range of PCB mount coaxial connectors and its dimensions are available at http://www.sriconnectorgage.com/pages/products/sma/smac.asp.

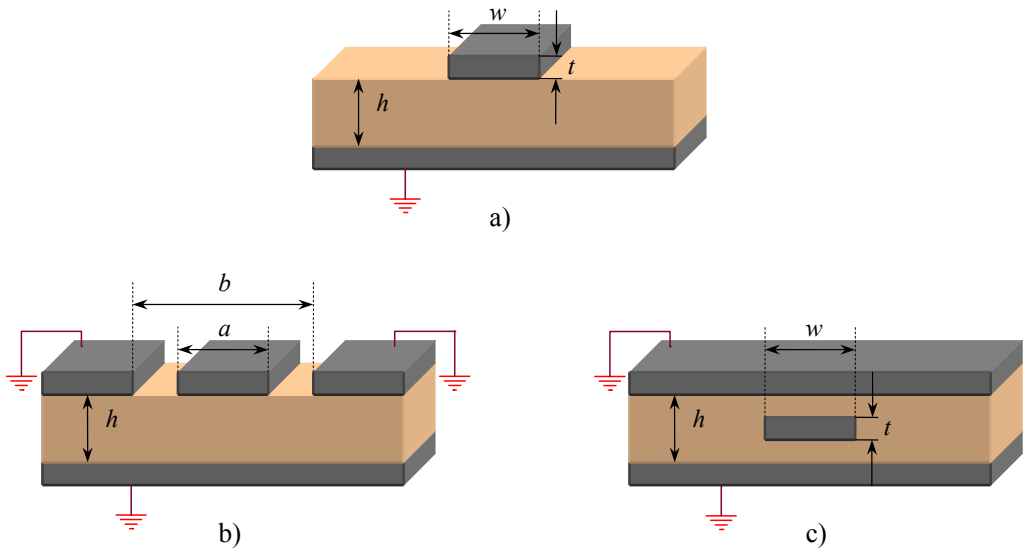


Figure 3.5. A cross-section view of the three kinds of PCB TLs considered a) microstrip b) coplanar waveguide with ground, and c) stripline.

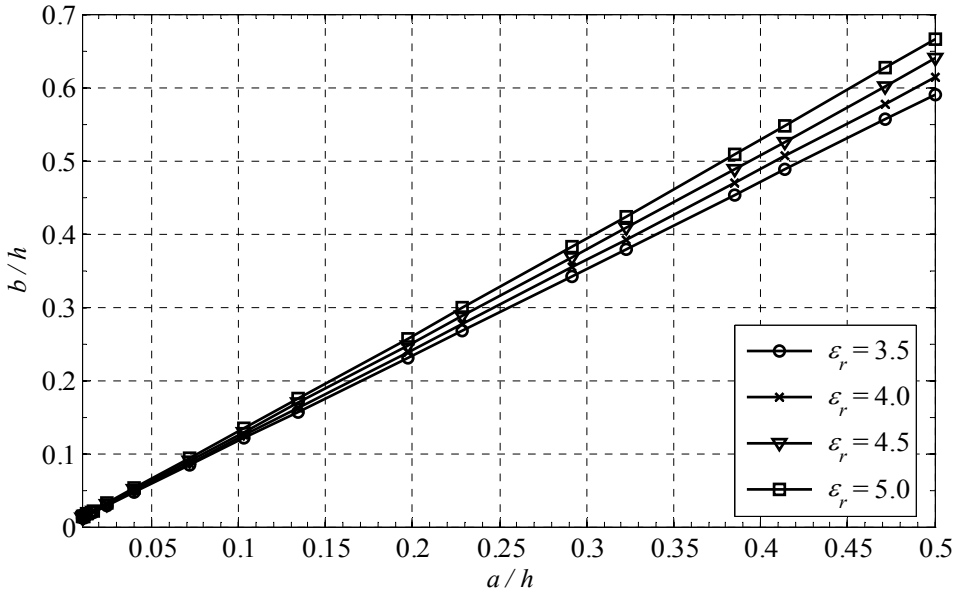


Figure 3.6. Required dimensions of a coplanar waveguide with ground in order to ensure a characteristic impedance of 50 Ω.

3.6 Conclusion

This chapter justified the design approach that will be applied to this dissertation in order to achieve an optimal design and accurate results. An overview of the design methodology was first given followed by a discussion around the IC manufacturing process. A description of the relevant CAD tools was then presented to emphasize and justify usage. Important considerations around the measurement setup that would ensure reliable and accurate measurement results were then pointed out. The dissertation can now proceed with a detailed description of the complete circuit design.

4.1 Introduction

Chapter 3 described the design methodology that was used in order to transform the literature review described in chapter 2 into a functional circuit. This approach was applied and the design, simulation and layout of a prototype circuit are now presented. The presentation and evaluation of the measurement results are discussed in the following chapter. This chapter starts off by examining the characteristics of the active and passive devices that could be used in the IC design. The system designs of the main components are then presented. This is then followed by a discussion on how all of these components were integrated into one complete design. The IC design phase is concluded by a discussion on the IC layout and floor planning. The design of the PCB is then presented.

4.2 NPN HBT small size and high frequency characteristics

To aid with circuit design, important conclusions about small size NPN transistors as well as its high frequency characteristics were needed. General assumptions about these transistors do not accurately describe the abovementioned conditions anymore. Although all hand-calculations were verified by simulations in the end, a more accurate description of the transistor behaviour under these conditions was needed to speed up the design process. Since there were no test circuits immediately available for measurements, these conclusions were drawn based on the compact simulation models as well as process parameters provided by the foundry.

The simulated transconductance for the NPN transistors at 5 GHz is shown in Figure 4.1. This was obtained by applying a small AC voltage signal at the base-emitter terminals of the transistor and then measuring the resulting AC current signal at the collector terminal. The simulation was repeated for different values of DC collector current. From the bipolar model presented in Figure 3.2a), the transconductance is approximated to be

$$g_m = \frac{I_C}{V_T}, \tag{4.1}$$

where

$$V_T \approx 26 \text{ mV} \text{ at } 300 \text{ °K}. \tag{4.2}$$

The quantity V_T is known as the thermal voltage and I_C denotes the DC collector current. By comparing equation (4.1) with Figure 4.1, the transconductance should have been approximately 20 mS when $I_C = 500$ µA at 300 °K. This approximation worsens for smaller emitter sizes and is at about 35 % in error for an emitter area $A_E = 1.2$ µm^2 when $I_C = 800$ µA. Therefore based on the compact model simulation results, the graph in Figure 4.1 should rather be used instead of equation (4.1) when selecting I_C to obtain the required transconductance when A_E is small.

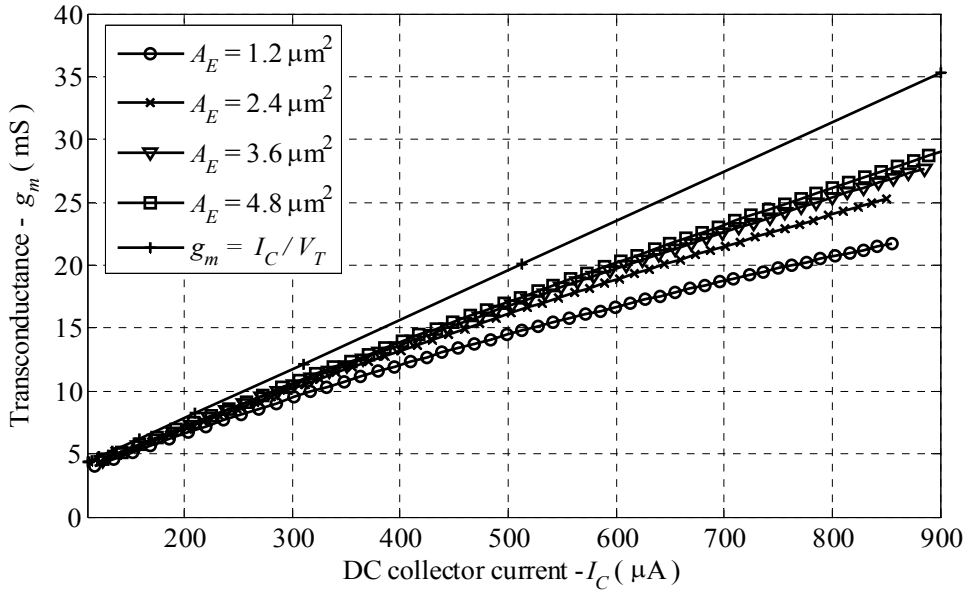


Figure 4.1. The transconductance of a high speed double base NPN HBT for various emitter sizes with $V_{CE} = 2$ V at 5 GHz along with its approximation.

The reduction in transconductance for small area emitters stems from the relation between the emitter resistance R_E and emitter area given by (Ashburn, 2003:107)

$$R_E \propto \frac{1}{A_E}, \tag{4.3}$$

and is around 25 Ω for a 0.4 µm^2 emitter (Austriamicrosystems AG, 2005a:24). A better approximation for the transconductance is derived by placing R_E in series with the emitter in Figure 3.2a). By solving this circuit the transconductance is more accurately expressed as

$$g_m \approx \frac{I_C}{V_T + I_C R_E}. \tag{4.4}$$

A simulated frequency sweep of the NPN with $A_E = 1.2\ \mu m^2$ over a range of I_C is shown in Figure 4.2. From the graph it can be seen that the transition frequency (f_t) varies between 17 and 64 GHz.

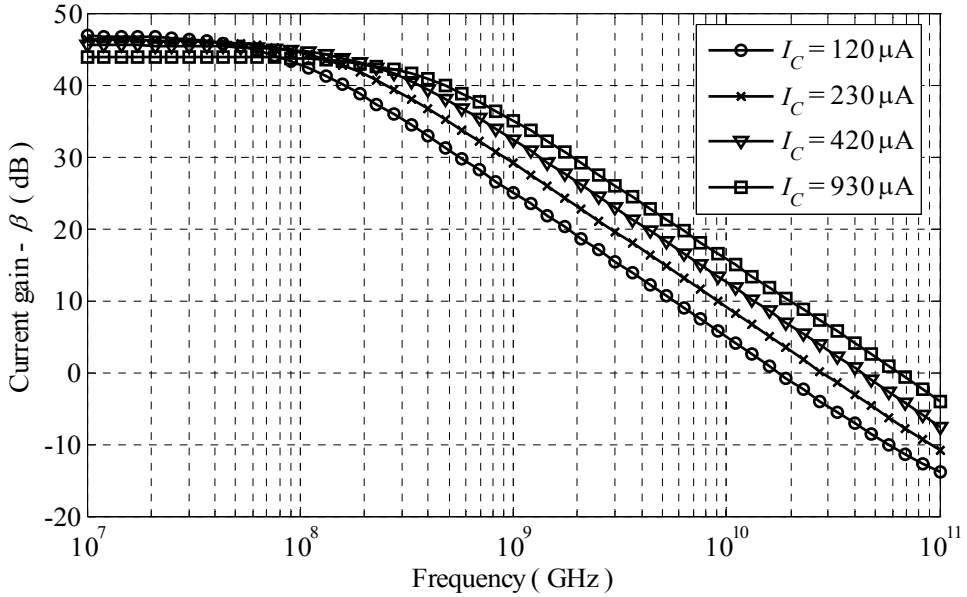


Figure 4.2. The simulated current gain as a function of frequency of a high speed double base NPN HBT for different values of I_C with $V_{CE} = 2$ V and $A_E = 1.2\ \mu m^2$.

An important conclusion that can be made from the graph in Figure 4.2 is that the common-emitter current gain at 5 GHz is only between 3.6 and 12. An estimation of the sum of the base-emitter capacitance C_π and the base-collector capacitance C_μ is given as (Gray, 2001:35)

$$C_\pi + C_\mu = \frac{g_m}{2\pi f_t} \approx 48\ \text{f F}\,. \tag{4.5}$$

4.3 MOSFET short channel and high frequency characteristics

Similar to the NPN transistors, general assumptions about the MOSFET transistors at low frequencies and in cases where the gate lengths are considered long do not hold under the opposite conditions. An expression of the drain current for a long channel MOSFET in the active region is given by

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS})\,, \tag{4.6}$$

where

- μ_n is the carrier mobility,
- C_{ox} is the gate-oxide capacitance per area,
- W and L are the gate width and length respectively,
- V_{GS} and V_{DS} are the gate-source and gate-drain voltage respectively,
- V_{TH} is the threshold voltage, and
- λ is the channel length modulation parameter.

A vertical electric field originating from the gate voltage forces the carriers in the channel closer to the surface of the silicon. The surface imperfections of the silicon impede the movement of the carriers which reduces its mobility (Gray, 2001:65). The carrier mobility in equation (4.6) that was derived from the total carrier concentration should be replaced by an effective carrier mobility given by

$$\mu_{n,eff} = \frac{\mu_n}{1+\theta(V_{GS}-V_{TH})} \tag{4.7}$$

where θ ranges from 0.1 V^{-1} to 0.4 V^{-1} for a gate-oxide thickness of 10 nm. The precise value is determined from a best fit based on the measured device characteristics.

Equation (4.6) was also derived assuming that

$$v_d = \mu_n E\,, \tag{4.8}$$

where v_d is the carrier drift velocity and E is the horizontal electric field between the drain and the source. Equation (4.8) is only valid when $v_d << v_{scl}$, where v_{scl} is the scattering limited velocity and is approximately 10^7 cm/s for silicon (Sze, 1985:61). A more accurate expression for the carrier drift velocity is given by

$$v_d = \frac{\mu_n E}{1+E/E_c} \tag{4.9}$$

where E_c is the electric field density where the carrier velocity is a factor of two less than equation (4.8) would have predicted. As the channel length gets smaller, the electric field density increases.

When the electric field density approaches E_c, equation (4.6) is no longer valid. Using equations (4.7) and (4.9), the drain current of a short channel MOSFET in the active region is approximated by (Gray, 2001:62)

$$I_D \approx \frac{\mu_{n,eff} C_{ox}}{2\left(1+\frac{V_{GS}-V_{TH}}{E_c L}\right)} \frac{W}{L}(V_{GS}-V_{TH})^2, \tag{4.10}$$

and the transconductance is given by

$$g_m = WC_{ox} v_{scl} \frac{\sqrt{1+\frac{2(V_{GS}-V_{TH})}{E_c L}}-1}{\sqrt{1+\frac{2(V_{GS}-V_{TH})}{E_c L}}}. \tag{4.11}$$

Assuming that $C_{gs} >> C_{gb} + C_{gd}$, the transition frequency now is given by

$$f_T = \frac{g_m}{2\pi C_{gs}} \propto \frac{v_{scl}}{L} \tag{4.12}$$

where C_{gs} is the gate-source capacitance, C_{gb} is the gate-bulk capacitance and C_{gd} is the gate-drain capacitance. It is worth comparing equation (4.12) to an expression of the transition frequency for a long channel MOSFET as given by

$$f_T = 1.5\frac{\mu_n}{2\pi L^2}(V_{GS}-V_{TH}). \tag{4.13}$$

From this it can be concluded that the transition frequency of the short channel MOSFET no longer depends on the overdrive voltage V_{GS} - V_{TH}, and no more reduces by a factor of L^2 but rather by a factor of only L.

In order to verify the design equations that were to be used for hand calculations, the characteristics of a MOSFET were simulated and plotted on the same axes as predicted by equation (4.6) and equation (4.10). Because PMOS transistors were also used, the simulation of this transistor is now presented. Table I lists the characteristics of this transistor as specified in the process parameters (Austriamicrosystems AG, 2005a:13).

Figure 4.3 compares simulated data with approximations given by equation (4.6) and equation (4.10). From this graph it is concluded the long channel approximation for a gate length of 0.35 µm is no longer valid when the source-gate voltage is higher than 1.2 V. The short channel approximation closely fits the simulated data and is only lower by a factor of $(1 + \lambda V_{DS})$ which was not included in equation (4.10).

TABLE I
CHARACTERISTICS OF A PMOS TRANSISTOR USED TO VERIFY SHORT CHANNEL MOSFET DESIGN EQUATIONS

Parameter	Value
W	5 µm
L	0.35 µm
C_{ox}	4.54×10^{-7} F/cm^2
μ_p	260 cm^2/V.s
$\mu_{p,eff}$	126 cm^2/V.s
E_c	3.846×10^{6} V/m
V_{TH}	0.68 V
v_{scl}	10^7 cm/s

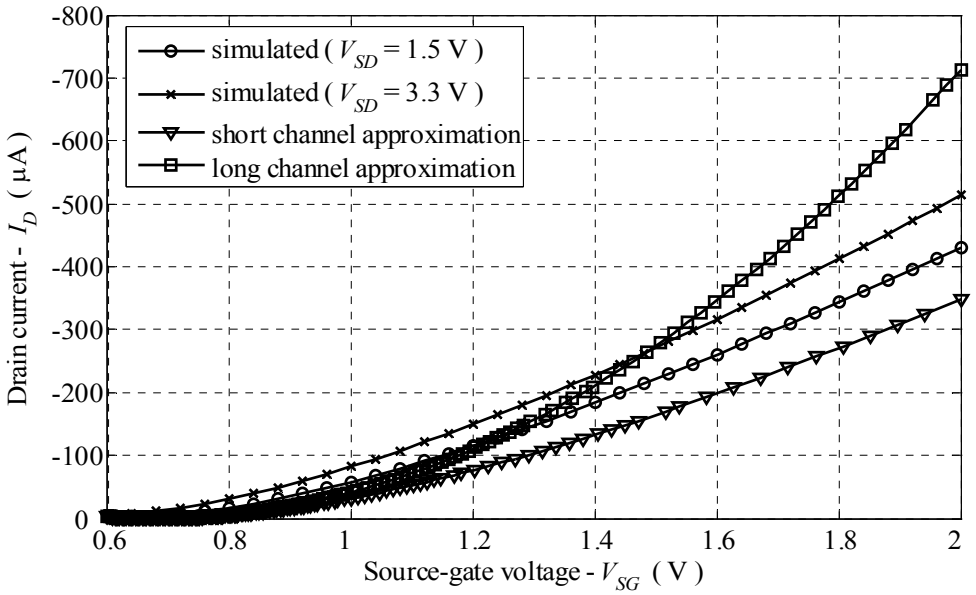


Figure 4.3. The simulated drain current vs. source-gate voltage of a short channel MOSFET along with its short and long channel approximations.

A simulated frequency sweep of the PMOS transistor that was characterized in Table I is shown in Figure 4.4. From this graph it can be concluded the transition frequency reaches a maximum as the drain current is increased. This can also be shown from equation (4.11) and equation (4.12) since

$$\lim_{V_{GS}\to\infty} g_m = WC_{ox}v_{scl}, \tag{4.14}$$

and therefore

$$\lim_{I_D \to \infty} f_T = \frac{3v_{scl}}{4\pi L} \approx 68 \text{ GHz}, \tag{4.15}$$

which is also an overestimate of the transition frequency because the gate-bulk and gate-drain capacitances were neglected from the equation. A more realistic approximation also takes into account that the gate-source voltage is limited by the specific process to 3.3 V. This results in

$$f_T\big|_{V_{GS}=3.3\text{V}} \approx 37 \text{ GHz}. \tag{4.16}$$

The simulated common-source current gain as a function of frequency for the PMOS transistor described in Table I is plotted in Figure 4.4. From this graph the transition frequency is approximately 18 GHz for $V_{GS} = 2.5$ V and was predicted to be approximately 32 GHz by equation (4.13).

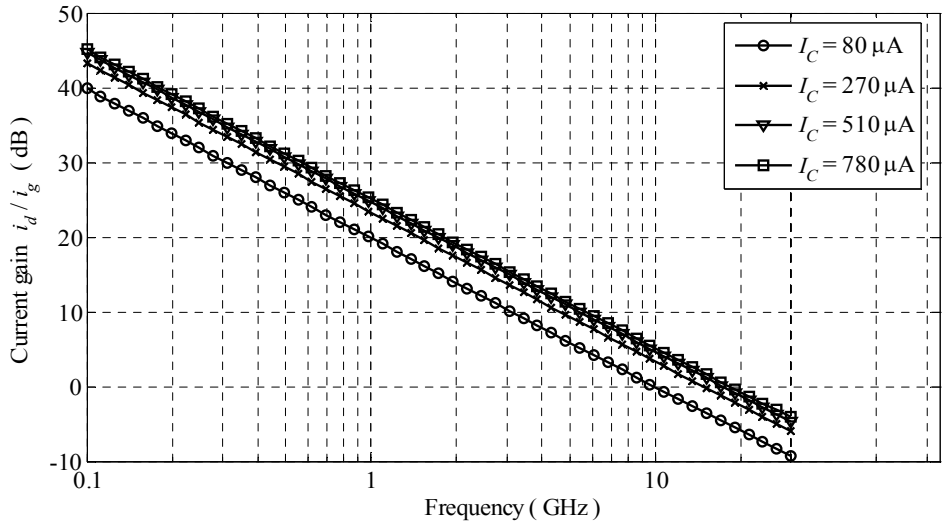


Figure 4.4. The simulated current gain as a function of frequency for a PMOS transistor width $W = 5$ µm and $L = 0.35$ µm.

4.4 Characterizing passive elements

In order to obtain the differential characteristics of the *LC*-tank circuit used in the oscillator, the linear 2-port network of the tank was simulated using SpectreRF. Even though the simulation was done using the PSP analysis, the *Z*-parameters are easily obtained by using conversion formulas (Pozar, 2005:187). The PSP simulation circuit setup is illustrated in Figure 4.5.

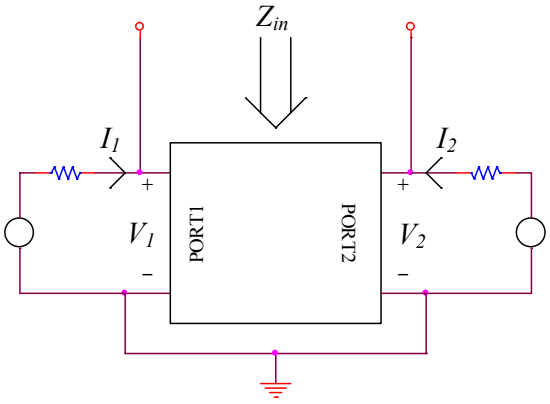


Figure 4.5. A test circuit to determine the differential input impedance and *Q*-factor using PSP simulations.

By removing the test sources and solving the voltage loop, the differential input impedance is given as

$$Z_{in} = \frac{V_1 - V_2}{I_1} = \frac{V_2 - V_1}{I_2} = \frac{V_1}{I_1} + \frac{V_2}{I_2}, \tag{4.17}$$

with

$$I_1 = -I_2. \tag{4.18}$$

The port voltages are defined as

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ -I_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} -I_2 \\ I_2 \end{bmatrix}, \tag{4.19}$$

which gives

$$\frac{V_1}{I_1} = Z_{11} - Z_{12}, \tag{4.20}$$

$$\frac{V_2}{I_2} = Z_{22} - Z_{21}. \tag{4.21}$$

Substituting (4.20) and (4.21) into (4.17) gives the differential input impedance as

$$Z_{in} = Z_{11} + Z_{22} - Z_{12} - Z_{21}. \tag{4.22}$$

For an inductive impedance the inductance is given by

$$L = \frac{\mathrm{Im}(Z_{in})}{2\pi f}, \tag{4.23}$$

and for a capacitive impedance the capacitance is

$$C = -\left[\mathrm{Im}(Z_{in})2\pi f\right]^{-1}. \tag{4.24}$$

The quality factor for both cases is defined as

$$Q = \left| \frac{\mathrm{Im}(Z_{in})}{\mathrm{Re}(Z_{in})} \right|. \tag{4.25}$$

These equations are now used to characterize the passive elements using PSP simulations.

Junction varactors from the Austriamicrosystems design kit were used for capacitive tuning. The tuning characteristics of the MOS varactor and the junction varactor at 5 GHz are shown in Figure 4.6.

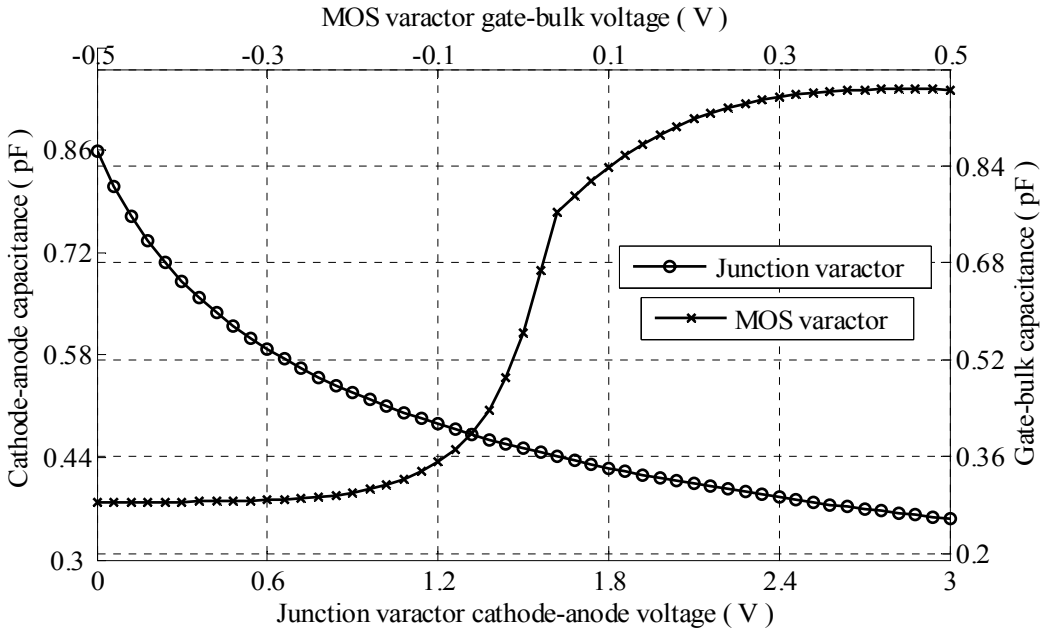


Figure 4.6. The simulated capacitance-voltage tuning characteristics of a 250 × 5 μm^2 junction varactor and a 317 × 0.65 μm^2 MOS varactor.

Even though the tuning range of the junction varactor is less when compared to the MOS varactor, the slope of the junction varactor is smaller when compared to that of the MOS varactor which allows for finer frequency tuning. The minimum and maximum capacitance for both devices scales linearly with the device dimensions. A *Q*-factor graph for the junction varactor is plotted in Figure 4.7. Since the characteristics of the junction varactor are very dependant on its cathode-anode voltage, this graph was plotted as a function of the tuning voltage instead of frequency. From Figure 4.7 it is seen that the smallest varactor will achieve the highest *Q*-factor.

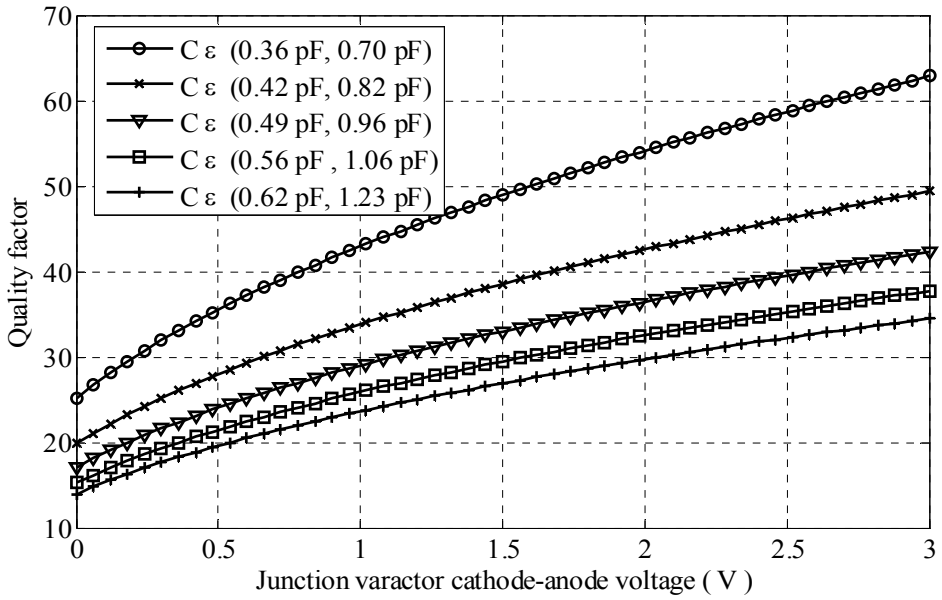


Figure 4.7. The simulated quality factor versus cathode-anode voltage of the 5 smallest junction varactors at 5 GHz available from the foundry.

Differential inductors also from the Austriamicrosystems design kit were used in the *LC*-tank of the VCO. The coupling between the differential inductors provides an improvement in the *Q*-factor of the tank (Danesh *et al.*, 1998). It is also useful in order to isolate the RF signal from the DC supply and occupies less space than two separate inductors. A frequency sweep of the available differential inductors around the frequency of interest is shown in Figure 4.8 and Figure 4.9.

The penalty for achieving higher inductance is an increase in the physical inductor layout dimensions and therefore only inductors smaller than 300 × 300 μm^2 were considered. The larger inductors achieved the highest *Q*-factors at the frequency of interest. This is not true in general however because the *Q*-factor of the smaller inductors peak at much higher frequencies than does the larger inductors.

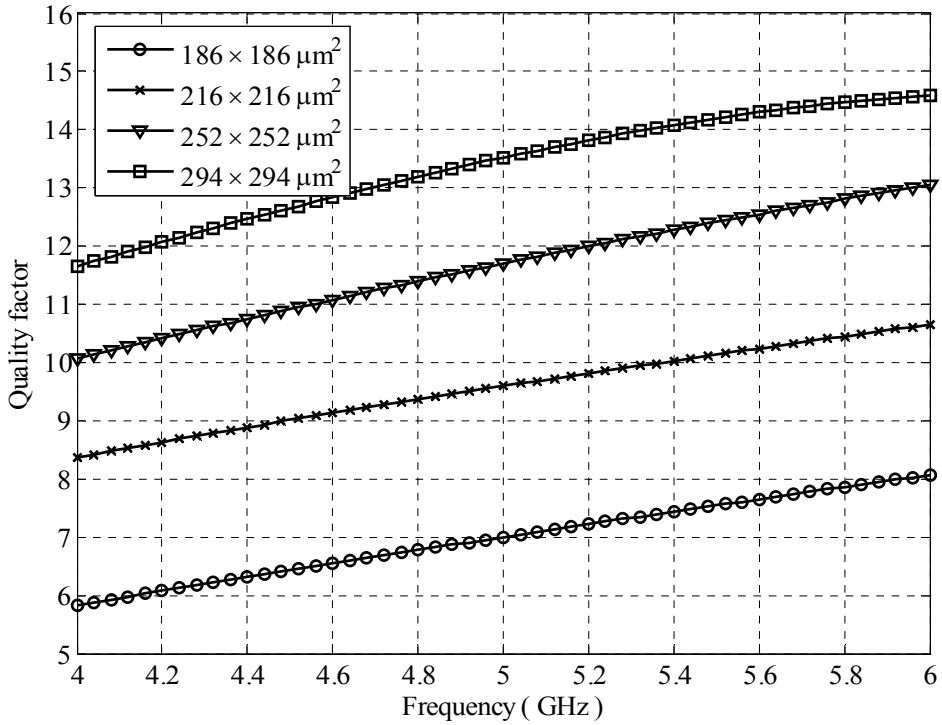


Figure 4.8. The simulated quality factor versus frequency of the 4 smallest inductors available from the foundry.

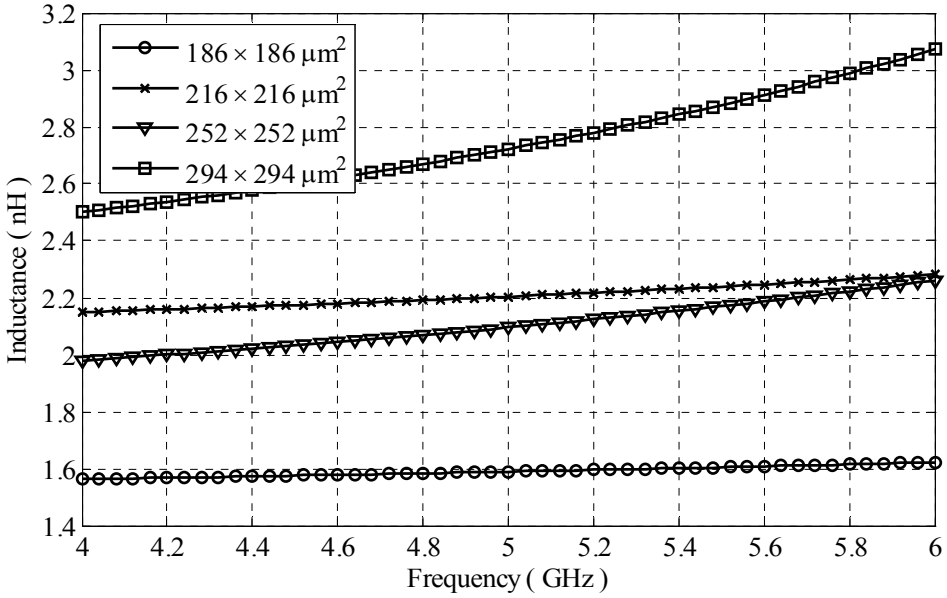


Figure 4.9. The simulated inductance versus frequency of the 4 smallest inductors available from the foundry.

4.5 Quadrature *LC*-VCO

The Quadrature *LC*-VCO topology to be used is shown in Figure 4.10 and was adapted from (Kakani, Dai and Jaeger, 2007) as discussed in section 2.3. The modification was to bias the bases of $Q_{1\text{-}4}$ using diodes $D_{1\text{-}8}$ instead of resistors. It was found that the phase noise improved considerably due to the reduction in the number of thermal noise sources. The purpose of diodes $D_{13\text{-}16}$ is to lower the V_{CE} of $Q_{10\text{-}15}$, which must be smaller than 2 V to avoid reverse breakdown (Austriamicrosystems AG, 2005a:7).

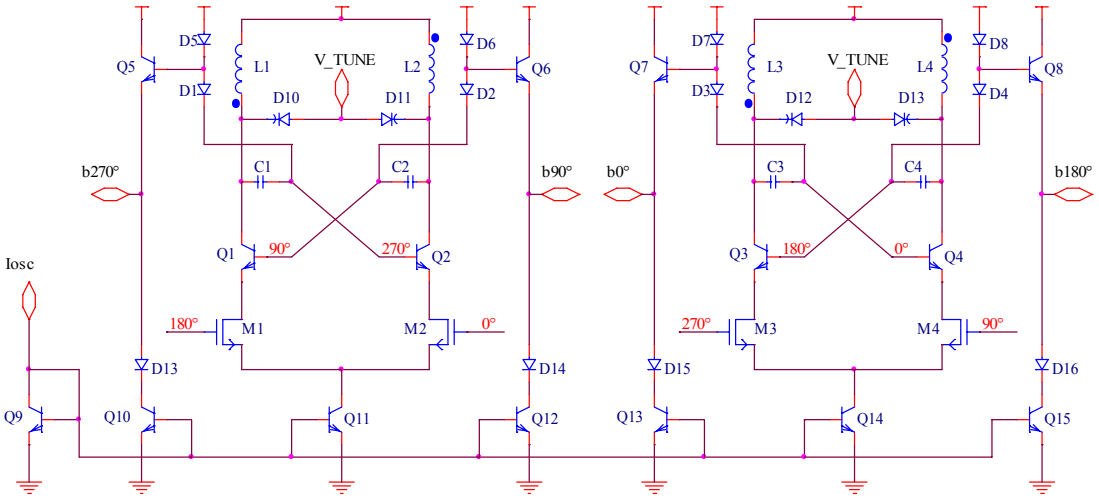


Figure 4.10. A circuit diagram of the Quadrature *LC*-VCO implementation.

The NMOS coupling transistors $M_{1\text{-}4}$ were designed so their transconductance is about the same as that of the bipolar transistors. Using equation (4.1) and equation (4.11) the width of these transistors are given by

$$W = \frac{I_C}{V_T C_{ox} v_{scl}} \frac{\sqrt{1+\frac{2(V_{GS}-V_{TH})}{E_c L}}}{\sqrt{1+\frac{2(V_{GS}-V_{TH})}{E_c L}}-1} \approx 0.192 I_C , \tag{4.26}$$

where the dimensions of W is (m) and the values for C_{ox}, v_{scl}, E_c, and L are given in Table I, $V_{GS} = 2$ V, $V_{TH} = 0.5$ V and I_C is the collector current of $Q_{1\text{-}4}$ in Figure 4.10.

The two main priorities in the design of the Quadrature *LC*-VCO were to achieve low phase noise and low power consumption. The two most significant factors that influence the phase noise are the tank voltage swing and the tank quality factor (Tiebout, 2005:28).

The two trade-offs involved here are the power dissipation which is dependant on the tank voltage swing, and the chip area which is dependant on the tank quality factor.

The approach taken was to first select the right combination of inductors and capacitors that were characterized in section 4.4 which would resonate over the specified frequency range. The combination with the highest resonating *Q*-factor would then be selected. The inductors and capacitors that were characterized in section 4.4 can be expressed with a resistance element in series with a reactive element. For the tank the capacitors and inductors are connected in parallel and the lumped circuit model is presented in Figure 4.11.

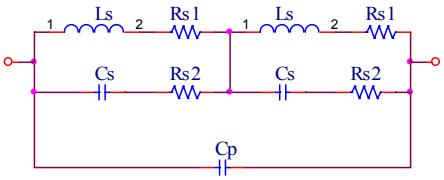


Figure 4.11. A lumped circuit model of the tank circuit.

By using Figure 4.8, Figure 4.9 and equation (4.25) L_s and R_{s1} at 5 GHz are tabulated in Table II. Similarly, by using Figure 4.6, Figure 4.7 and equation (4.25) C_s and R_{s2} at 5 GHz are tabulated in Table III. In this table R_{s2min} represents the series resistance when the capacitance is at its lowest and vice versa for R_{s2max}. Because the centre-tap of the inductor is connected to the AC ground, the values for L_s and R_{s1} are halves of the total series inductance and resistance respectively. Capacitor C_p was added to model the parasitic capacitance of the active circuit and is around 200 fF (Kakani, Dai and Jaeger, 2007). The parallel resonance frequency of the tank was obtained by solving

$$\frac{\partial}{\partial \omega}\left[2\left(j\omega L_s + R_{s1}\right) \| \left(-j/\omega C_s + R_{s2}\right)\right] \| C_p = 0\,. \tag{4.27}$$

Since the complex impedances cancel each other at the resonant frequency, equation (4.25) cannot be used to find the *Q*-factor of the tank anymore. The *Q*-factor is instead defined by

$$Q = \frac{f_{res}}{f_{c,high} - f_{c,low}}, \tag{4.28}$$

where f_{res} is the resonant frequency found using equation (4.27) and $f_{c,high}$ and $f_{c,low}$ are the upper and lower cutoff frequencies respectively. More specifically $f_{c,high}$ and $f_{c,low}$ are the frequencies where the tank impedance is -3 dB lower than the impedance at resonance.

TABLE II
THE LUMPED CIRCUIT PARAMETERS OF THE FOUR SMALLEST INDUCTORS AVAILABLE FROM THE FOUNDRY.

Dimensions (μm^2)	L_s (nH)	R_{s1} (Ω)
186 × 186	0.80	3.59
216 × 216	1.10	3.64
252 × 252	1.05	2.81
294 × 294	1.35	3.03

TABLE III
THE LUMPED CIRCUIT PARAMETERS OF THE FIVE SMALLEST JUNCTION VARACTORS.

Dimensions (μm^2)	C_{smin} (pF)	R_{s2min} (Ω)	C_{smax} (pF)	R_{s2max} (mΩ)
250 × 1.4	360	3.54	700	721
300 × 1.4	420	3.79	820	776
350 × 1.4	490	3.82	960	789
400 × 1.4	560	3.79	1100	790
450 × 1.4	620	3.67	1200	739

From Table II and Table III and using equation (4.27) and equation (4.28), the resonant frequencies and *Q*-factors for different combinations of inductors and capacitors can be obtained at both ends of the tuning range. These resonant frequencies and *Q*-factors are presented in Table IV and Table V respectively. In these tables headings A – D represent combinations between inductors with dimensions 186 × 186 μm^2, 216 × 216 μm^2, 252 × 252 μm^2, 294 × 294 μm^2 respectively, and the corresponding junction varactor. These inductors are from here on referred to by these corresponding table headings. The combinations that achieve a frequency range over the design specifications are highlighted in gray.

From Table IV and Table V the two most suitable combinations are the 250 × 1.4 μm^2 varactor in parallel with either inductor B or C. The *Q*-factor of the resonating tank when using inductor C is 22 % higher compared to inductor B. The trade-off however is that inductor C is 36 % larger than inductor B. This cost must be justified when comparing the phase noise performance obtained between these two inductors.

TABLE IV
THE TANK RESONANT FREQUENCIES FOR FIVE DIFFERENT VARACTORS CONNECTED IN PARALLEL WITH THE FOUR SMALLEST INDUCTORS.

Varactor size (μm^2)	A (GHz)	B (GHz)	C (GHz)	D (GHz)
250 × 1.4	5.36 ~ 6.46	4.58 ~ 5.51	4.68 ~ 5.64	4.13 ~ 4.97
300 × 1.4	5.09 ~ 6.22	4.34 ~ 5.30	4.45 ~ 5.43	3.92 ~ 4.78
350 × 1.4	4.82 ~ 5.97	4.11 ~ 5.09	4.21 ~ 5.21	3.71 ~ 4.59
400 × 1.4	4.59 ~ 5.75	3.92 ~ 4.90	4.01 ~ 5.02	3.54 ~ 4.42
450 × 1.4	4.45 ~ 5.58	3.79 ~ 4.75	3.88 ~ 4.87	3.42 ~ 4.29

TABLE V
THE TANK *Q*-FACTORS FOR FIVE DIFFERENT VARACTORS CONNECTED IN PARALLEL WITH THE FOUR SMALLEST INDUCTORS.

Varactor size (μm^2)	A	B	C	D
250 × 1.4	6.94 ~ 7.40	8.05 ~ 8.58	9.97 ~ 10.32	10.55 ~ 11.02
300 × 1.4	6.50 ~ 6.81	7.53 ~ 7.91	9.29 ~ 9.41	9.84 ~ 10.08
350 × 1.4	6.09 ~ 6.31	7.05 ~ 7.33	8.68 ~ 8.66	9.20 ~ 9.30
400 × 1.4	5.75 ~ 5.91	6.66 ~ 6.87	8.18 ~ 8.07	8.68 ~ 8.68
450 × 1.4	5.58 ~ 5.66	6.47 ~ 6.57	7.95 ~ 7.71	8.43 ~ 8.30

Phase noise simulations for the 250 × 1.4 μm^2 varactor in parallel with inductors B and C are shown in Figure 4.12 and Figure 4.13 respectively. The phase noise was calculated at a 1 MHz offset from the carrier and swept over a range of bias currents. The simulation was repeated for different values of varactor tuning voltages and the corresponding oscillating frequencies f_{res}, are presented in the legends of the graphs.

From Figure 4.12 the optimum bias current would be at approximately 3.6 mA to achieve an overall maximum phase noise of -113 dBc / Hz. In comparison with Figure 4.13 the optimum bias current for the larger inductor is lower at 2.8 mA to achieve an overall maximum phase noise of -115 dBc / Hz. The oscillation frequency for this structure however does not fall into specified frequency range. The oscillation frequency can on the other hand be increased by reducing C_p through reducing the width of the coupling transistors $M_{1\text{-}4}$. This solution was however not approached since it was already decided that the 36 % increase in inductor dimensions would not justify the 2 dB reduction in phase noise nor the 22 % reduction in power consumption. For the final oscillator the magnitude

of the oscillating voltage Δv_{osc}, between nodes b0° and b180° in Figure 4.10 was found to be 430 ~ 584 mV over the entire varactor tuning range for the bias current set to 3.5 mA.

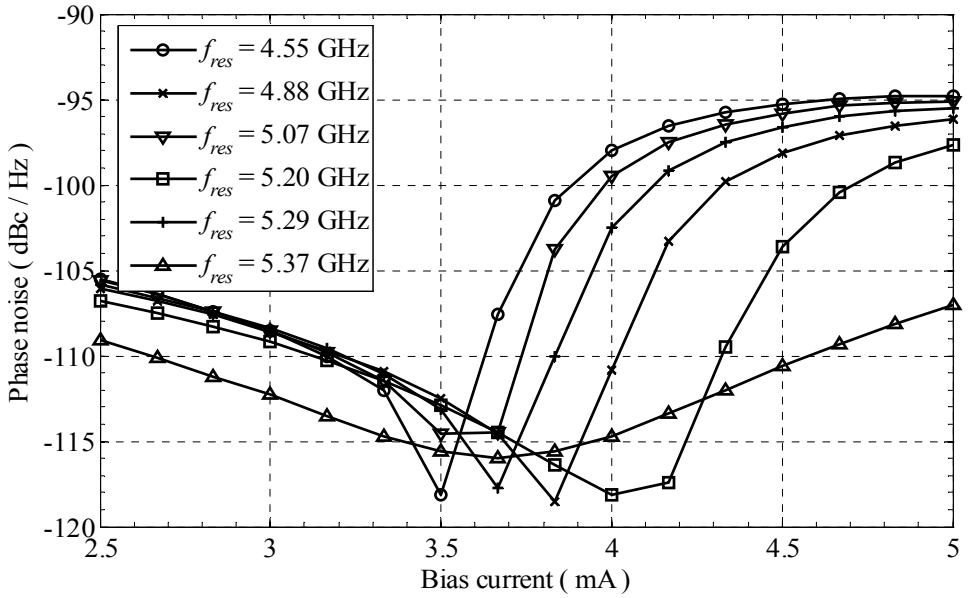


Figure 4.12. Simulated phase noise @ 1 MHz offset of the oscillator for a 250 × 1.4 μm^2 varactor in parallel with inductor B.

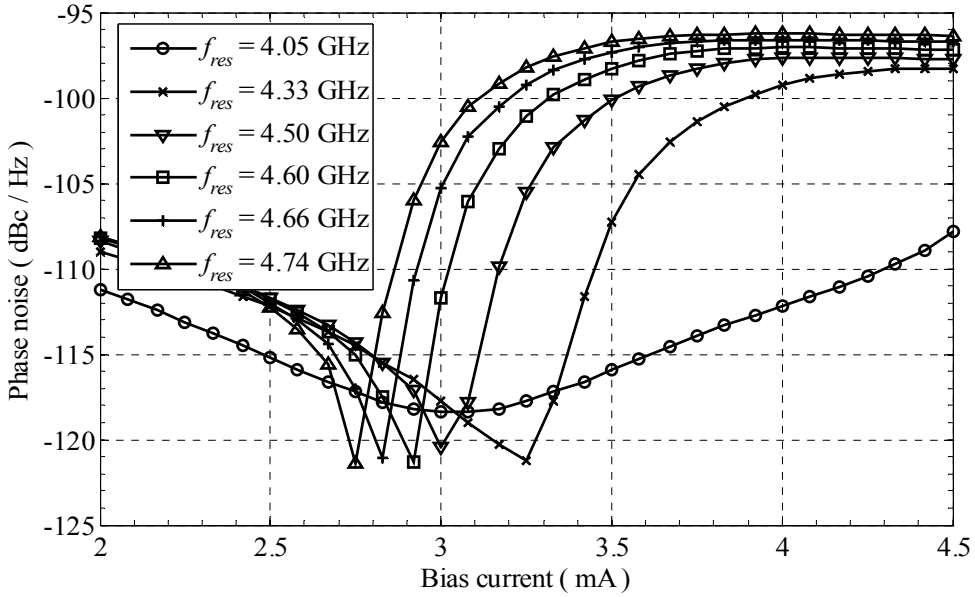


Figure 4.13. Simulated phase noise @ 1 MHz offset of the oscillator for a 250 × 1.4 μm^2 varactor in parallel with inductor C.

4.6 VGA

The VGA was implemented using a modified Gilbert mixer cell as shown in Figure 4.14. Resistors $R_{3\text{-}6}$ were added to the mixer cell in order to expand its dynamic range (Sansen and Meyer, 1974). $Q_{20\text{-}21}$ and $Q_{22\text{-}23}$ are Darlington pairs and their purpose are twofold. Firstly, they provide $2V_{BE}$ DC voltage drops that are necessary to allow sufficient voltage swing required by the Gilbert mixer cells. Secondly they increase the β of the transistors which is already as low as 10 at around 5 GHz. The RF signal generated by the oscillator is applied at V_{2+} and V_{2-}. $Q_{16\text{-}17}$ act as a differential voltage-to-current converter (Gray, 2001:715). $R_{1\text{-}2}$ are emitter degeneration resistors that increase the input impedance of V_{2+} and V_{2-} and linearise the large signal input from the quadrature LC-VCO. $Q_{18\text{-}19}$ form part of a pre-distortion circuit that compensates for the non-linearity of $Q_{24\text{-}25}$. $Q_{30\text{-}34}$ are current sources used for biasing.

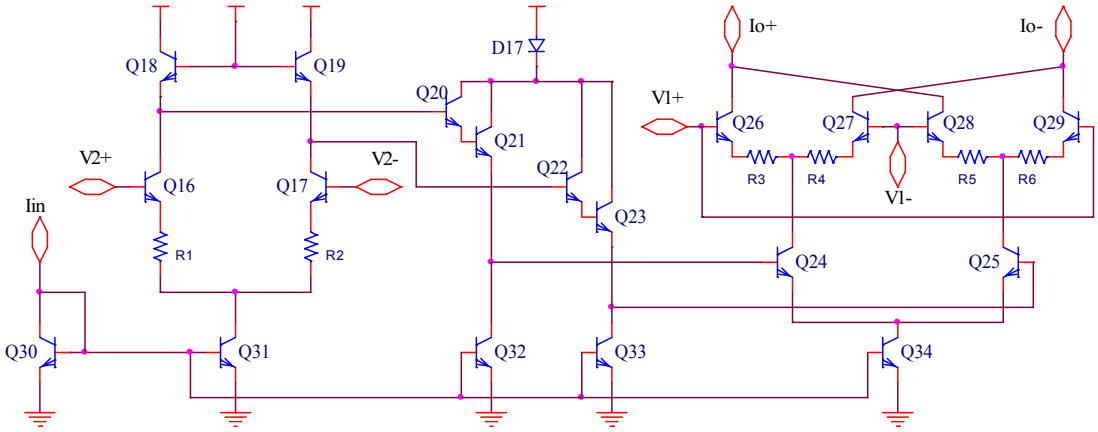


Figure 4.14. A circuit diagram of the VGA implementation.

The differential collector current of $Q_{16\text{-}17}$ can be estimated by

$$\Delta i_{C16-17} \approx \frac{\alpha g_m}{\alpha + g_m R_E} \Delta v_2 , \tag{4.29}$$

where $\alpha = \beta/(\beta + 1)$[5] and $R_E = R_1 = R_2$. Since a higher DC current increases the current gain, there is a trade-off between current gain and power dissipation. Because of the finite and relatively low value of β, the loading of the oscillator at the bases of $Q_{16\text{-}17}$ was examined. Since $i_{b16} = -i_{b17}$ and $\Delta i_b = \Delta i_c/\beta$ the differential input impedance can be written as

[5] Note that in most cases $\alpha \approx 1$ but this is not accurate when $\beta \approx 6$.

$$R_{id,VGA} = \frac{\Delta v_2}{i_b} = 2\left(\frac{\beta}{g_m} + (\beta + 1)R_E\right). \tag{4.30}$$

In order to minimize the oscillator current load, the condition $R_{id,VGA} >> R_{out,osc}$ should hold. A good starting point is to choose $\beta/g_m = 500\ \Omega$. From Figure 4.1 and Figure 4.2 a value for $I_{C16\text{-}17} = 400\ \mu A$ would satisfy this condition. The current source Q_{31} is therefore set to $I_{C31} = 800\ \mu A$.

Because the input signal from the oscillator $\Delta v_{osc} \approx 400$ mV, the non-linear large signal characteristics of the HBTs are expected to introduce significant harmonic distortion on the differential collector current of $Q_{16\text{-}17}$. With the addition of $R_{1\text{-}2}$, a portion of Δv_{osc} drops across these resistors which causes the base-emitter voltage signals of $Q_{16\text{-}17}$ to be reduced. This not only linearises the collector currents but also reduces the transconductance by a factor of $(1 + g_m R_E/\alpha)$ as seen from equation (4.29). To analyze the effect of this linearization the first harmonic and the second harmonic distortions are simulated and plotted in Figure 4.15 as a function of $R_{1\text{-}2}$ when $\Delta v_2 = 400$ mV. From this analysis it can be seen that when $R_{1\text{-}2} > 200\ \Omega$, the fundamental current starts declining significantly with the distortion not being reduced very much. The values of $R_{1\text{-}2}$ were therefore set to 140 Ω.

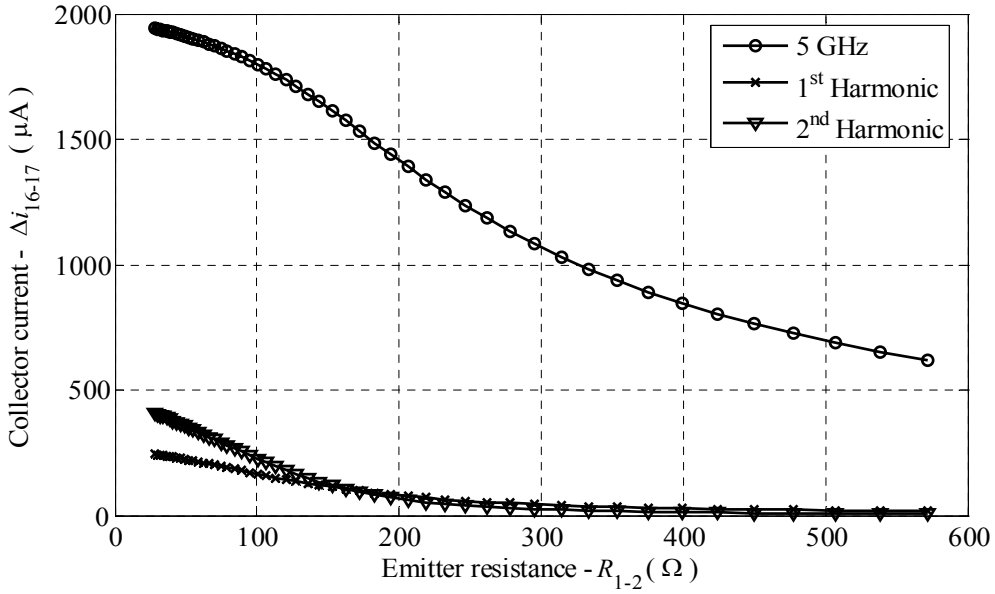


Figure 4.15. Fundamental differential collector current as well as the first and second harmonic distortion as a function of $R_{1\text{-}2}$ for $\Delta v_2 = 400$mV.

The differential collector voltage for transistors $Q_{18\text{-}19}$ is given by

$$\Delta v_{C18-19} = 2V_T \tanh^{-1}\left(\frac{\alpha g_m \Delta v_2}{(\alpha + g_m R_E) I_{C31}}\right). \tag{4.31}$$

If one assumes that the voltage drops across $Q_{20\text{-}23}$ remain constant, the differential voltage at the base of $Q_{24\text{-}25}$, $\Delta v_{b24\text{-}25} = \Delta v_{b18\text{-}19}$. The differential collector current at $Q_{24\text{-}25}$ is now given by

$$\Delta i_{c24-25} = I_{C34} \tanh\left(\frac{\Delta v_{b24-25}}{2V_T}\right) = \frac{I_{C34}}{I_{C31}} \frac{\alpha g_m \Delta v_2}{\alpha + g_m R_E} = K_1 \Delta v_2 , \tag{4.32}$$

with

$$K_1 = \frac{I_{C34}}{I_{C31}} \frac{\alpha g_m \Delta v_2}{\alpha + g_m R_E} \approx 2.03 I_{C34} \text{ A/V} , \tag{4.33}$$

for $\alpha = 6/7$, $g_m = 12$ mS and $\Delta v_2 = 400$ mV.

For the case where $R_{3\text{-}6} = 0\ \Omega$, the differential output current is given by

$$\Delta i_o = \Delta i_{c24-25} \tanh\left(\frac{\Delta v_1}{2V_T}\right) = K_1 \Delta v_2 \tanh\left(\frac{\Delta v_1}{2V_T}\right). \tag{4.34}$$

When $\Delta v_1 << V_T$, equation (4.34) can be approximated by

$$\Delta i_o \approx \frac{K_1}{2V_T} \Delta v_1 \Delta v_2 \approx 38.75 I_{C34} \Delta v_1 \text{ A} . \tag{4.35}$$

In order to maximize the high current gain, $I_{C34} = 1.33$ mA was selected for the current source Q_{34}.

For the case when $R_{3\text{-}6} > 0\ \Omega$, there exists no closed form solution like that of equation (4.34) (Gray, 2001:217). The effect of these resistors is therefore simulated over a range of values and plotted in Figure 4.16. As was mentioned earlier, the idea behind the addition of these resistors was to expand the input tuning range of the mixer, allowing much more accurate and stable phase tuning. A side effect of this solution is that the current gain was reduced. It was decided that $R_{3\text{-}6} = 180\ \Omega$ would be a reasonable trade-off.

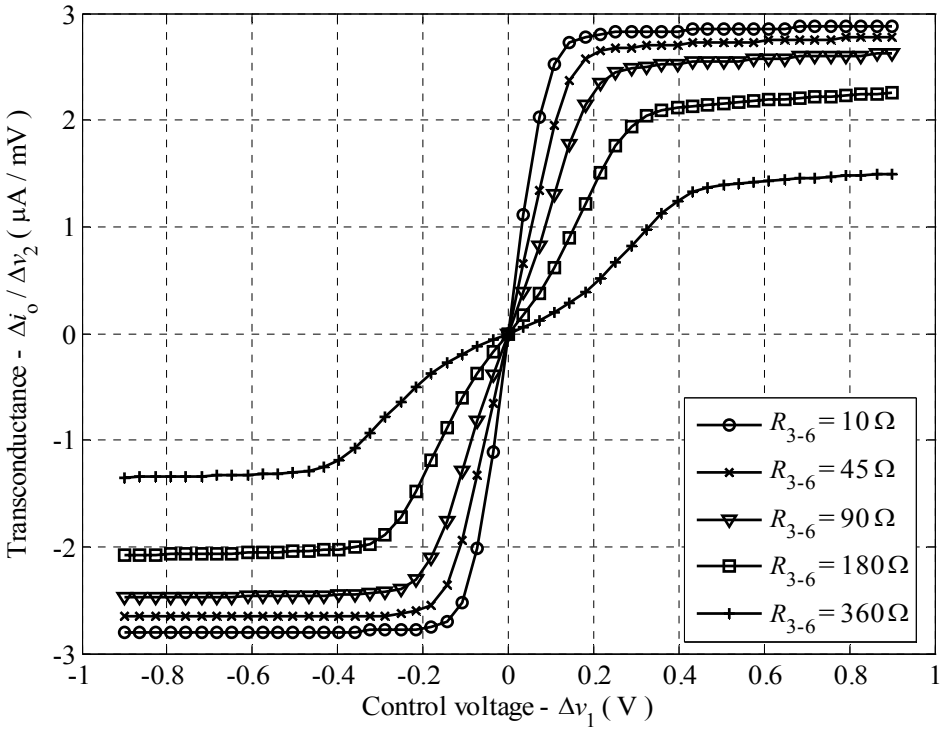


Figure 4.16. Simulated transfer curve of the Gilbert mixer at 5 GHz, illustrating the effect of adding emitter degeneration resistors to the mixer cell.

4.7 Current mirror

The purpose of the current mirror is to transform a differential current into a single ended voltage. The current mirror is the last stage required in order to obtain the final phase shifted signal. As mentioned in Chapter 2, this signal can be used at the input of a modulator/demodulator or a PA stage before transmission. This research does not focus the design of either stages and therefore the current mirror also serves as the final output stage of the design.

Before the transformation the differential currents are first added together, which realizes the vector sum as discussed in section 2.2. A circuit diagram of the current mirror is shown in Figure 4.17. $M_{5\text{-}6}$ both consist of multiple 5×0.35 μm^2 transistors connected in parallel in a multifingered layout and the total width of both transistors are the same. The output is obtained at the drain of M_6 and is given by

$$v_{sd6} = \sqrt{\Delta i_{o(I)}^2 + \Delta i_{o(Q)}^2}\left.\frac{\partial v_{sd6}}{\partial i_{d6}}\right|_{I_{D6}=I_{C34}} . \quad (4.36)$$

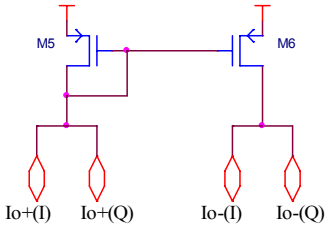


Figure 4.17. A circuit diagram of the current mirror implementation.

Equation (4.14) shows that in order to maximize the high frequency current gain, the source-gate voltage needs to be maximized. This maximum value is however limited by the minimum collector-emitter voltages of $Q_{24\text{-}29,34}$ including the voltage drops across $R_{3\text{-}6}$ in Figure 4.14. The DC source-gate voltage is then

$$V_{SG} = \left(V_{DD} - V_{BE34} - V_{BE24-25} - V_{BE26-29} - I_{C34} \times R_{3-6}/2\right) + 10\ \% \approx 1.24\ \text{V} \quad (4.37)$$

where $V_{DD} = 3.3$ V and $V_{BE24\text{-}24,34} \approx 0.7$ V when $V_I = 0$ V and $I_{o+} = I_{o-} = 0.5I_{C34} = 0.66$ mA.

The DC transfer curve of the source-drain voltage vs. the drain current for different values of source-gate voltages is plotted in Figure 4.18. The transistor's characteristics are the same as the one characterized in Table I. For $V_{SG} = 1.24$ V, $I_{D5} \approx 130$ µA / gate as read off from Figure 4.18. The number of gates was chosen to be 10 so that $I_{D5} \approx 1.3$ mA. From equation (4.36) and Figure 4.18

$$v_{sd6} \approx 50 \times 10^3 \times \Delta i_o \ \text{A} \quad (4.38)$$

for this configuration.

Equation (4.36) assumes that there are no parasitic capacitances influencing the transconductance of the PMOS transistors. This assumption can be justified by looking at the location of the pole of the current mirror given as (Gray, 2001:532)

$$|p_1| = \frac{g_{m5}}{2C_{gs}} = \frac{3v_{scl}\left(\sqrt{1+\frac{2(V_{GS}-V_{TH})}{E_c L}}-1\right)}{4L\sqrt{1+\frac{2(V_{GS}-V_{TH})}{E_c L}}} = 55.97 \times 10^9 \ \text{rad/s} \quad (4.39)$$

using equation (4.9), Table I and $V_{SG} = 1.24$ V. The cutoff frequency caused by the pole is

$$F_{c,mirror} = \frac{|p_1|}{2\pi} = 8.91 \text{ GHz}. \quad (4.40)$$

Since the cutoff frequency is higher than the operating frequency, equation (4.38) is accurate for this case.

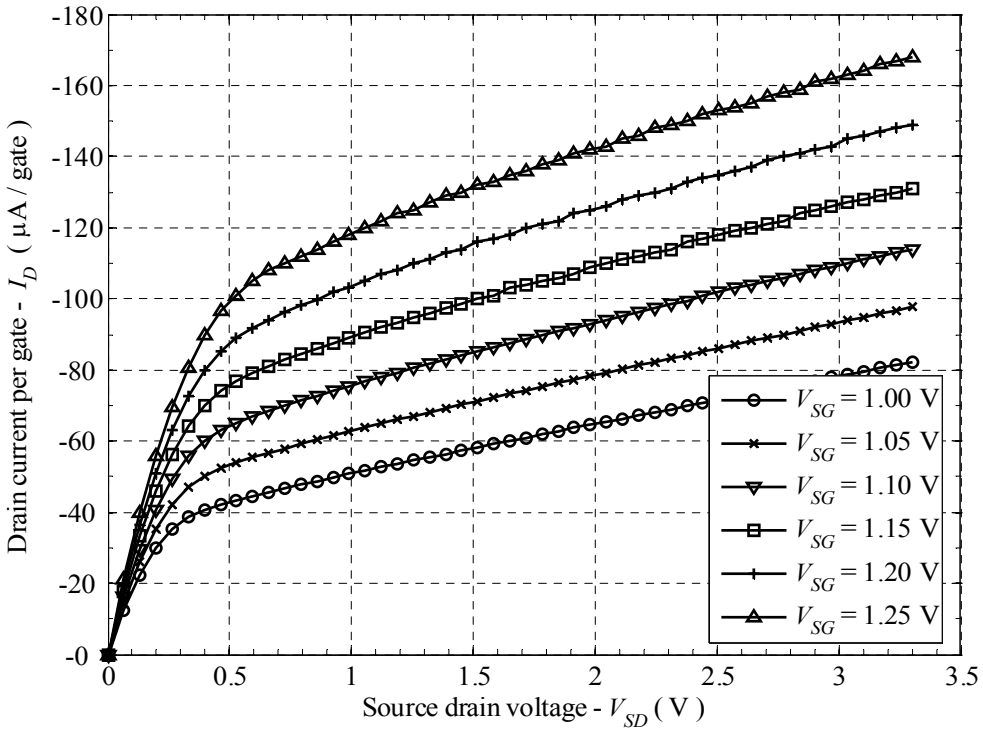


Figure 4.18. The drain current per gate vs. source-drain voltage of the PMOS used in the current mirror.

4.8 Bias circuitry

As was mentioned before, both the VCO and Gilbert mixer are biased using current sources. An 800 µA and a 355 µA current source were designed using PMOS transistors and Figure 4.19 shows a circuit schematic of these current sources.

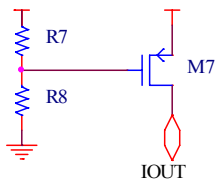


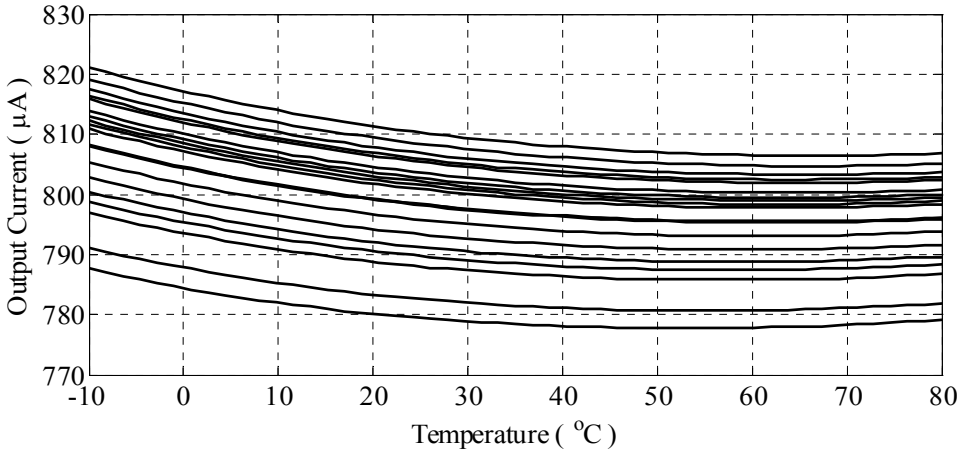
Figure 4.19. A circuit schematic PMOS current source.

Because the drain-current is dependant on the supply voltage, it is sensitive to power supply variations. This can also be shown by using equation (4.6) and ignoring the $(1 + \lambda V_{DS})$ factor to find that

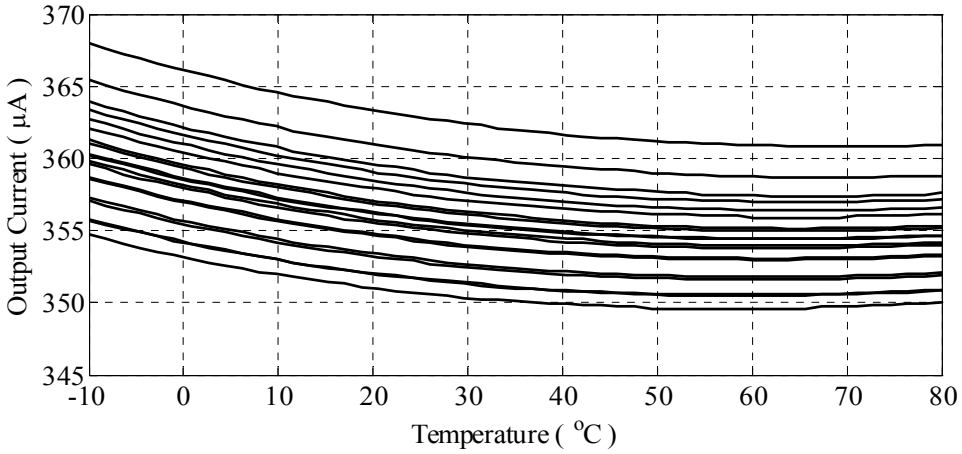
$$S_{V_{DD}}^{I_{OUT}} = \frac{V_{DD}}{I_{OUT}} \cdot \frac{\partial I_{OUT}}{\partial V_{DD}} = \frac{2V_{DD}}{V_{DD} - 2V_{TH}}, \tag{4.41}$$

where $S_{V_{DD}}^{I_{OUT}}$ is the sensitivity of I_{OUT} with respect to variations in V_{DD} and is 3.40 for this case. This means that an increase in V_{DD} of 1 % would increase I_{OUT} by 3.40 % for instance. There exist a number of circuits that can be used for power supply insensitive biasing (Gray, 2001:309). For this design however, a stable voltage supply was assumed and power supply insensitive biasing was not considered. The temperature sensitivity was however simulated through SPICE.

Resistors R_7 and R_8 are identical and are in the kΩ range, in order to minimize current consumption. The area of each resistor was chosen to be 25 × 5 μm^2 in order to minimize mismatching. Because both resistors are identical the gate of the PMOS is biased at ½V_{DD}. The main parameters that determine the drain current are V_{SD} and the W / L ratio. Since V_{BE} and V_{CE} of the NPN current mirrors is mostly around 0.7 V, V_{SD} is usually around 2.6 V. To ensure sufficient matching, the minimum gate area was selected to be 150 μm^2. For the 355 μA current source, W / L = 52.2 μm / 3 μm was found using equation (4.6) and then optimized using SPICE. Similarly for the 800 μA source, W / L = 117.6 μm / 3μm was found. Figure 4.20a) and b) show the variation in output current over temperature of 20 different samples for both the 800 μA and 355 μA current sources respectively. The samples were simulated in SPICE using a Monte Carlo sweep on the process parameters and layout matching. The deviations of both current sources as shown in Figure 4.20 are acceptable for the two circuit components that will be biased using these.



a)



b)

Figure 4.20. Simulated variation in output current for a) the 800 µA and b) the 350 µA over temperature for 20 different samples.

4.9 Digital phase tuner

The purpose of the digital phase tuner is to provide a digital interface that allows a discrete number of pre-defined phase shifts. Because of the non-linear transfer characteristic of the phase control inputs, this circuit makes phase shifting a lot easier and also enables the phase shift to be controlled by a digital processor. The difficulty with analogue phase tuning arises when a constant amplitude over the entire phase tuning range is desired. This is because of the relation

$$A_Q / A_I = \tan\varphi, \tag{4.42}$$

that has to be maintained over the entire phase tuning range. In equation (4.42), A_I and A_Q represent the in-phase and quadrature amplitudes respectively and φ represents the desired phase shift. The digital phase shifter was designed to enable discrete tuning between 16 different phases, equally spaced between 0 ° and 360 °.

As mentioned in section 4.7, the output voltage signal is generated at the drain of M_6 in Figure 4.17. Because this signal is directly proportional to input currents of both the quadrature and in-phase signals, their amplitudes must obey the relation given in equation (4.42). For a maximum current of 820 μA for both signals, the required amplitudes for the 16 different phases are shown in columns 2 and 4 of Table VI. In order to obtain the required voltage levels at V_{1+} of the VGA in Figure 4.14, the transfer function of the VGA is plotted in Figure 4.21 and used to read off the voltage levels. For this plot, V_{1-} is set to 1.9 V. The voltages obtained from Figure 4.21 are tabulated columns 3 and 5 of Table VI.

It can be seen from columns 3 and 5 of Table VI that there are only 8 different voltage levels required in order to select between 16 different phases. A simple DAC that delivers these 8 specific voltage levels was therefore designed and connected to V_{1+}. A circuit schematic of the DAC is shown in Figure 4.22. The same DAC was connected to V_{1-}, but this DAC was hard-wired so that it would always deliver 1.90 V. The amount of current flowing through R_9 is controlled by switching the gates of $M_{17\text{-}25}$ between 0 V and V_{BE}. R_9 was set to 1.2 kΩ with an area of 50 × 5 μm^2 which is large enough for good matching. The W/L of M_{17} was selected so that $V_{1+} = 2.23$ V when $\text{Control}_{\text{A-H}}$ is high. The gate dimensions of M_{18} was selected so that $V_{1+} = 2.18$ V when only $\text{Control}_{\text{A}}$ is low. Similarly, the gate dimensions of M_{19} was selected so that $V_{1+} = 2.11$ V when only $\text{Control}_{\text{A-B}}$ are low. The gate dimensions of $M_{20\text{-}25}$ were designed similarly so that all the required voltages are obtained as more Control signals are switched low, until $V_{1+} = 1.36$ V when $\text{Control}_{\text{A-H}}$ are all low.

The digital phase tuner consists of a digital decoder and two of the DACs described above. A functional diagram of the circuit is shown in Figure 4.23. One of the DACs was connected to V_{1+I} and the other to V_{1+Q}. The digital decoder must decode the 4-bit input signal and set the Control signals on both DACs, so that the corresponding voltage levels are obtained on the outputs of the DACs as listed in Table VI.

TABLE VI
THE REQUIRED OUTPUT CURRENTS FOR BOTH THE IN-PHASE AND QUADRATURE SIGNALS IN ORDER TO GENERATE SPECIFIC PHASE SHIFTS. THE CORRESPONDING CONTROL VOLTAGE LEVELS AT V_{1+} ARE ALSO GIVEN.

φ	$I_{max}\cos(\varphi)$ (µA)	ΔV_{1I} (mV)	$I_{max}\sin(\varphi)$ (µA)	ΔV_{1Q} (mV)
0 °	820	0.33	0	0.00
-22.5 °	758	0.28	-314	-0.13
-45.0 °	580	0.21	-580	-0.21
-67.5 °	314	0.13	-758	-0.29
-90.0 °	0	0.00	-820	-0.54
-112.5 °	-314	-0.13	-758	-0.29
-135.0 °	-580	-0.21	-580	-0.21
-157.5 °	-758	-0.29	-314	-0.13
-180 °	-820	-0.54	0	0.00
-202. 5 °	-758	-0.29	314	0.13
-225.0 °	-580	-0.21	580	0.21
-247.5 °	-314	-0.13	758	0.28
-270.0 °	0	0.00	820	0.33
-292.5 °	314	0.13	758	0.28
-315.0 °	580	0.21	580	0.21
-337.5 °	758	0.28	314	0.13

The digital decoder was designed in VHDL and an extract of the behavioural description code is given in Figure 4.24. The entire code is given in Appendix A. In this code *phaseSel* is the 4-bit input signal and *IPhase* and *QPhase* are the 8-bit output signals to the in-phase and quadrature DACs respectively. When *phaseSel* = '0000' the phase shift $\varphi = 0$ ° and *phaseSel* increments up to '1111' for $\varphi = -337.5$ °. The behavioural VHDL code was synthesized into a logic circuit using Precision RTL Synthesis from Mentor Graphics® together with the 3.3 V standard cell core libraries from Austriamicrosystems. The resulting logic circuit diagram of the digital decoder is also shown in Appendix A.

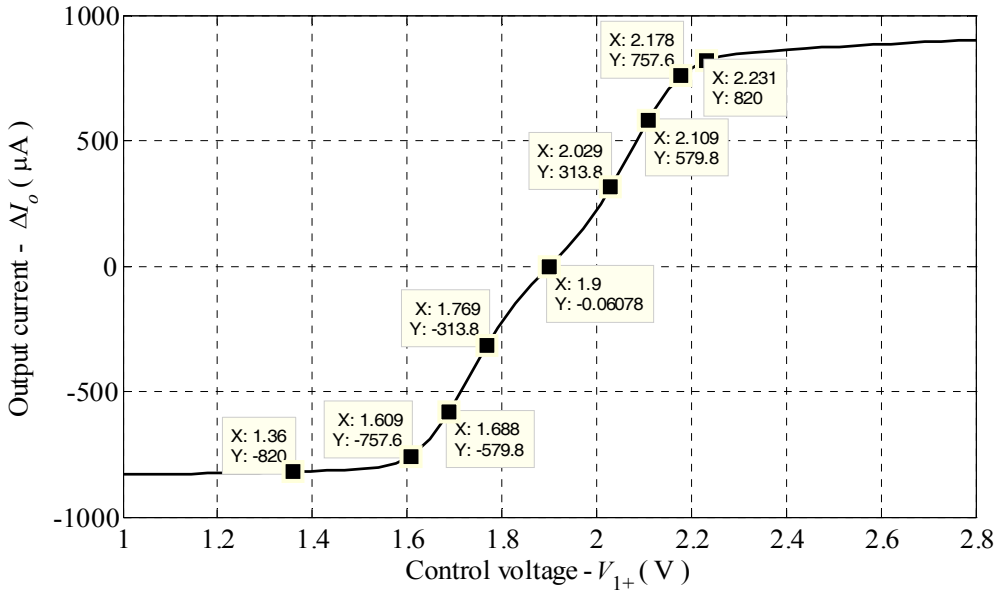


Figure 4.21. The simulated voltage-to-current transfer function of the VGA at 5 GHz.

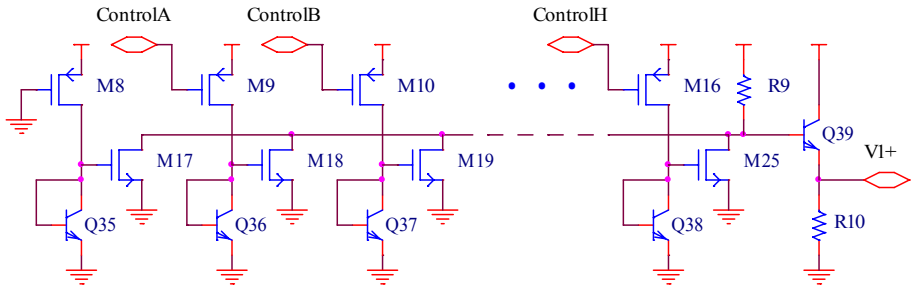


Figure 4.22. Circuit diagram of the DAC used.

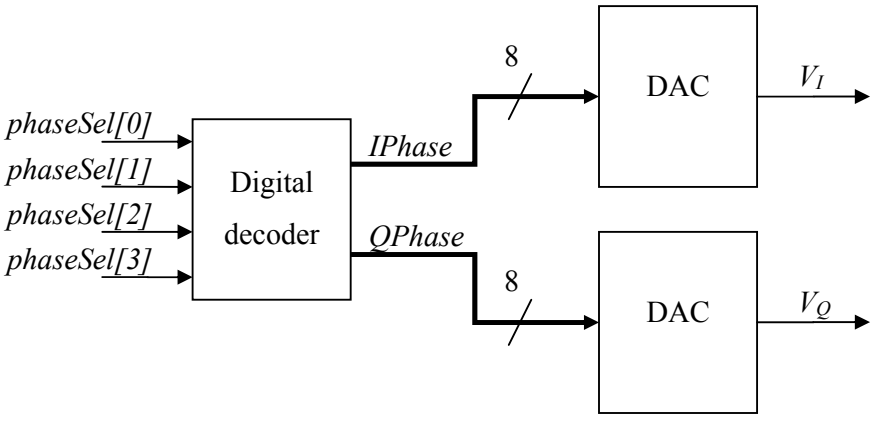


Figure 4.23. Functional diagram of the digital phase tuner.

```
case phaseSel is
when "0000" =>
IPhase<= "11111111";
QPhase<= "00001111";
when "0001" =>
IPhase<= "01111111";
QPhase<= "00011111";
                .
                .
                .
when "1110" =>
IPhase<= "00111111";
QPhase<= "00000011";
when "1111" =>
IPhase<= "01111111";
QPhase<= "00000111";
end case;
```

Figure 4.24. An extract of the VHDL code used to design the digital decoder.

4.10 Design integration

The complete design is shown in Figure 4.25. The IC was packaged in a QFN48 package and inductors $L_{5\text{-}9} = 1.2$ nH are included to model the bond wire inductance (Chen *et al.*, 2003) of the chip packaging. Capacitors $C_{5\text{-}9} = 1$ pF are for AC coupling to 50 Ω loads. The current mirror delivers approximately -17 dBm the each 50 Ω load, which is acceptable considering that a power amplification stage was not included and this power signal is 113 dBm higher than the noise floor of the measuring equipment that were used (Agilent Technologies, 2008a). The 4-bit phase shift is selected using phaseSel_A – phaseSel_D and Vtune is used to vary the frequency between 4.6 and 5.3 GHz.

For this design there are four phase shifters connected to the quadrature *LC*-VCO. In principle any number of phase shifters could be connected to the quadrature *LC*-VCO, as long as the loading effect by these devices is looked at. The output impedance of the oscillator along with its buffer stages is modelled with a resistor $R_{osc,out}$ in series with a capacitor $C_{osc,out}$. These values were obtained by loading each of the quadrature outputs of the oscillator with an ideal inductor using SPICE and sweeping its inductance until the current passing through it peaked. This peak current value through one of the outputs was

recorded as $i_{\max}$ and the corresponding inductance as L_{match}. The open-circuit voltage on one of the outputs was also simulated using SPICE and is recorded as v_{oc}.

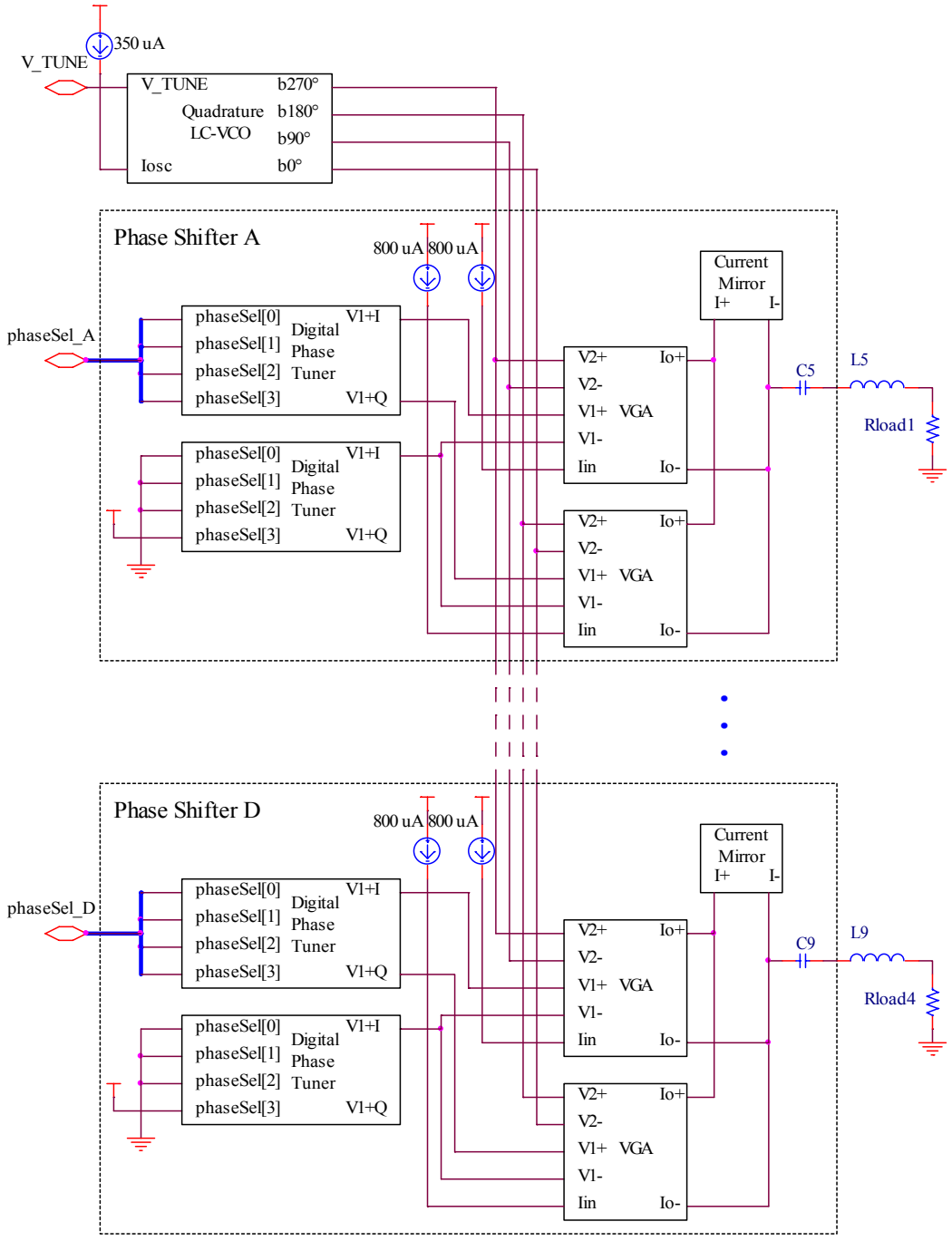


Figure 4.25. Circuit schematic of the entire design.

The differential output impedance between both 180 ° out of phase outputs is given as

$$R_{osc,out} = \frac{2v_{oc}}{i_{\max}} = \frac{530\ \text{mV}}{205\ \mu\text{A}} \approx 2.6\ \text{k}\Omega\,, \tag{4.43}$$

$$C_{osc,out} = \frac{1}{\omega^2 2L_{match}} = \frac{1}{(5\times10^9 \times 2\pi \text{ rad/s})^2 \times 2 \times 520 \text{ pH}} \approx 970 \text{ fF}, \quad (4.44)$$

over the entire operating frequency.

The input impedance of the VGA was also obtained through simulations. An AC voltage source with an amplitude $v_{in} = 400$ mV was applied to inputs V_{2+} and V_{2-} of the VGA. An inductor was placed in series with the voltage source and the VGA. The inductance was swept until there was no difference in phase between the voltage and current signals. The inductance was then noted as L_{match} and the current as $i_{\max}$. The differential input impedance is

$$R_{VGA,in} = \frac{v_{in}}{i_{\max}} = \frac{400 \text{ mV}}{1.4358 \text{ mA}} \approx 280 \ \Omega, \quad (4.45)$$

$$C_{VGA,in} = \frac{1}{\omega^2 L_{match}} = \frac{1}{(5\times10^9 \times 2\pi \text{ rad/s})^2 \times 50.3 \text{ nH}} \approx 20 \text{ fF}, \quad (4.46)$$

over the entire operating frequency.

The 1.9 V reference signal required at V_{1-} for every VGA is obtained using digital phase tuners. This was done so that variations in process parameters which might influence the value of this reference signal will also shift the x-axis of Figure 4.21 in a similar direction. Simulation results of the complete circuit are shown in Chapter 5.

4.11 IC layout and floor planning

The layout floorplan of the entire circuit is shown in Figure 4.26. Detailed individual layouts for each device can be found in Appendix B. Special effort was made to ensure that the design is symmetrical around both the vertical and horizontal axis. There are two layout versions for the digital phase tuner. The larger one is the original digital phase tuner as discussed in section 4.9. The smaller one is a modified version that only supplies a 1.9 V reference voltage. The purpose of this modified digital phase tuner was discussed in section 4.10. It is smaller than the original digital phase tuner because only the circuitry for the V_{1+I} output was laid out. The circuitry for digital decoder was also not included since the DAC was already hardwired to provide the 1.9 V output.

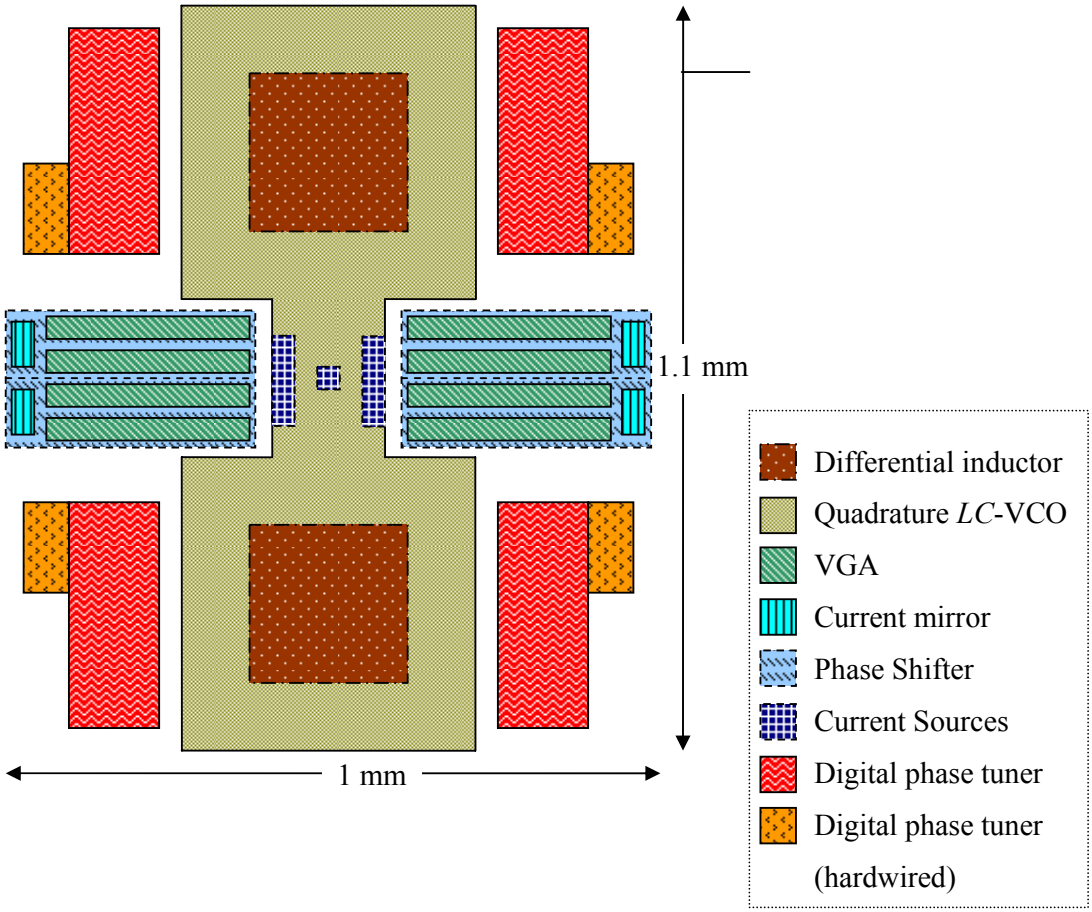


Figure 4.26. Layout floorplan of the entire design.

The concept layout floorplan shown in Figure 4.26 was however modified in order to make the measurement setup of the entire circuit more practical. Both versions of the digital phase tuner were moved away and disconnected from the rest of the circuit. The outputs of these devices were connected to output pins. Inputs V_{1+} and V_{1-} of the VGAs were connected to input pins. The VGAs and the digital phase tuners therefore had to be connected externally using the PCB. A restriction in the number of pins available only allowed two of the original digital phase tuners and one modified digital phase tuner to be used. These devices were therefore shared between all four phase shifters. This modification to the concept floorplan allowed the phase tuners to be measured using analogue input signals at V_{1+} as well, so that the performance of the phase shifter would not be subjected to the performance of the digital phase tuner. Another advantage of this modification is that there could now be experimented with continuous phase tuning as well.

Figure 4.27 shows the complete chip layout with its main components which are numbered from 1 to 6 in the figure itself and are as follows:

1. the layout of the complete circuit, excluding the digital phase tuner,
2. a Quadrature *LC*-VCO as discussed in section 4.5,
3. a single current mirror,
4. a VGA biased using an 800 µA current source,
5. two original digital phase tuners, and
6. a modified digital phase tuner.

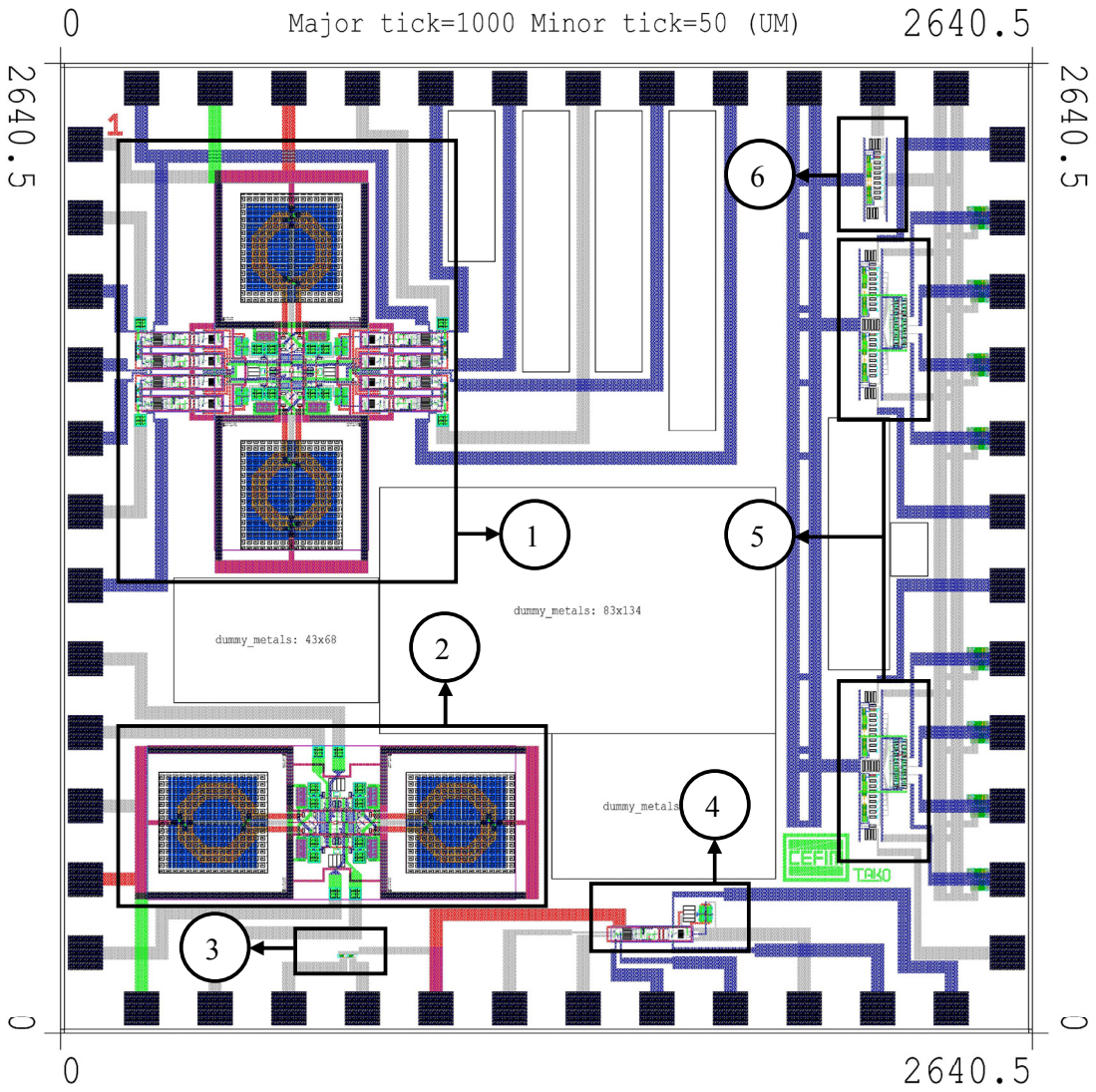


Figure 4.27. Complete chip layout.

Components 2, 3 and 4 are placed apart from the rest of the circuit and are powered using a separate supply line. These components are not powered when the entire design is being

measured and are separated only to allow them to be measured independently from the rest of the design.

The layouts of the individual components are shown in more detail in Appendix B. The entire layout was designed to be fitted into a QFN48 package provided by SEMPAC Inc. (Sempac Inc., 2008) and packaged through Europractice (Europractice, 2008). The dimensions of the die are 2640.5 × 2640.5 μm^2. Figure 4.28 shows a chip photograph of the manufactured design and the bonding diagram is shown in Appendix B.

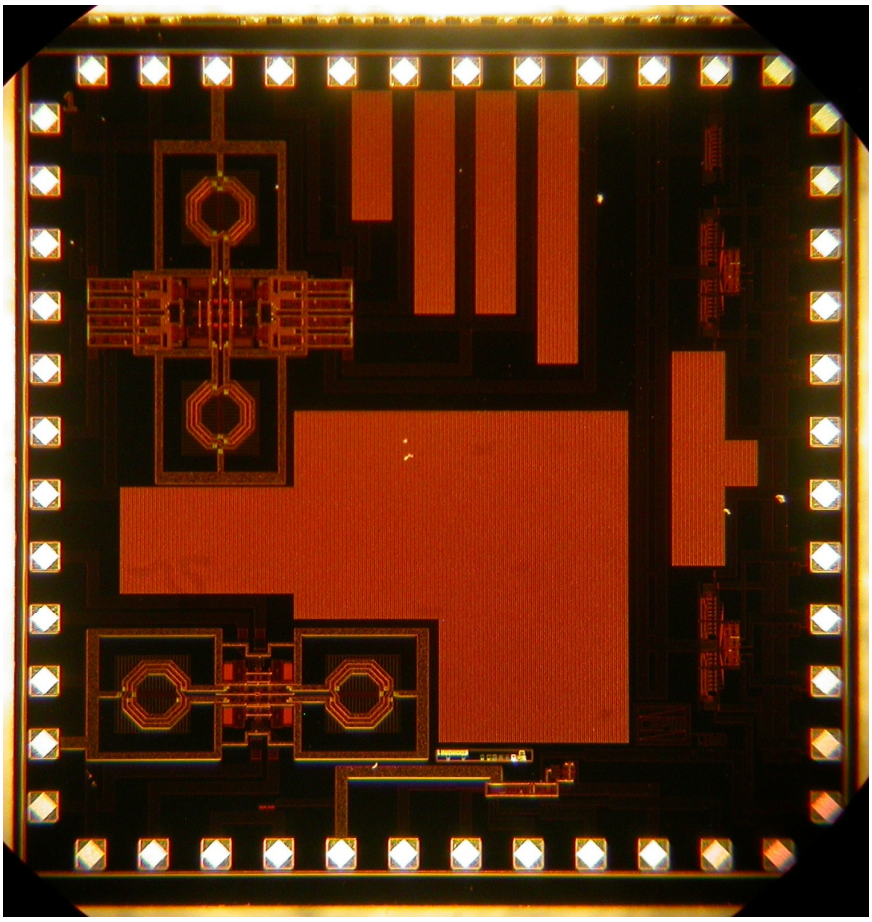


Figure 4.28. A chip photograph of the manufactured design.

4.12 Evaluation PCB design

The design of an evaluation PCB was outsourced to a third party company known as Avancé Technologies (Avancé Technologies., 2008). The PCB was designed based on the

schematic in Figure 4.29. SW1 and SW2 are used to control the 4-bit digital phase tuners. The analogue output signals from these devices are then connected to the rest of the design through JP1-JP4. Since the current flowing into the V_{1+} input of the VGAs is not significant, the resistance introduced by the bond wires and PCB tracks does not create significant voltage drops.

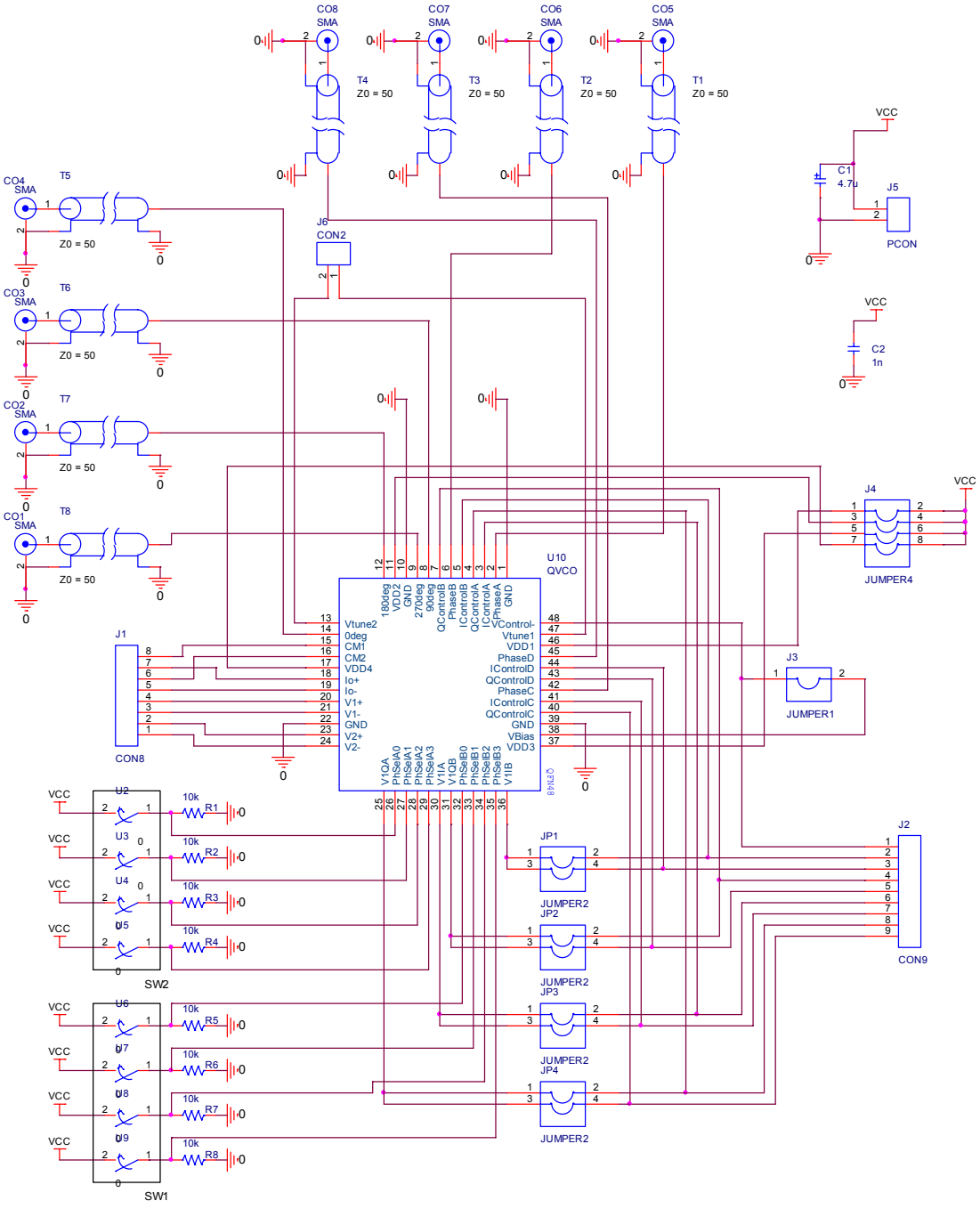


Figure 4.29. Schematic of the evaluation PCB.

The 1.9 V reference signal is connected to V_{1-} through J3. Different sections of the chip are powered separately using J4. The frequencies of both oscillators are tuned separately by connecting DC sources to J6. Connector J2 allows various DC analogue and digital signals to be probed. Capacitors C1 and C2 are added to suppress high frequency noise, but more capacitors were added at the discretion of the PCB designer, based on possible interferences between nearby tracks on the final PCB layout. T1-T8 are 50 Ω TLs that were design based on the discussion in section 3.5 and CO1-CO8 are 50 Ω SMA connectors used to connect the RF signals to the measurement equipment. A photograph of the PCB with its components populated is shown in Figure 4.30.

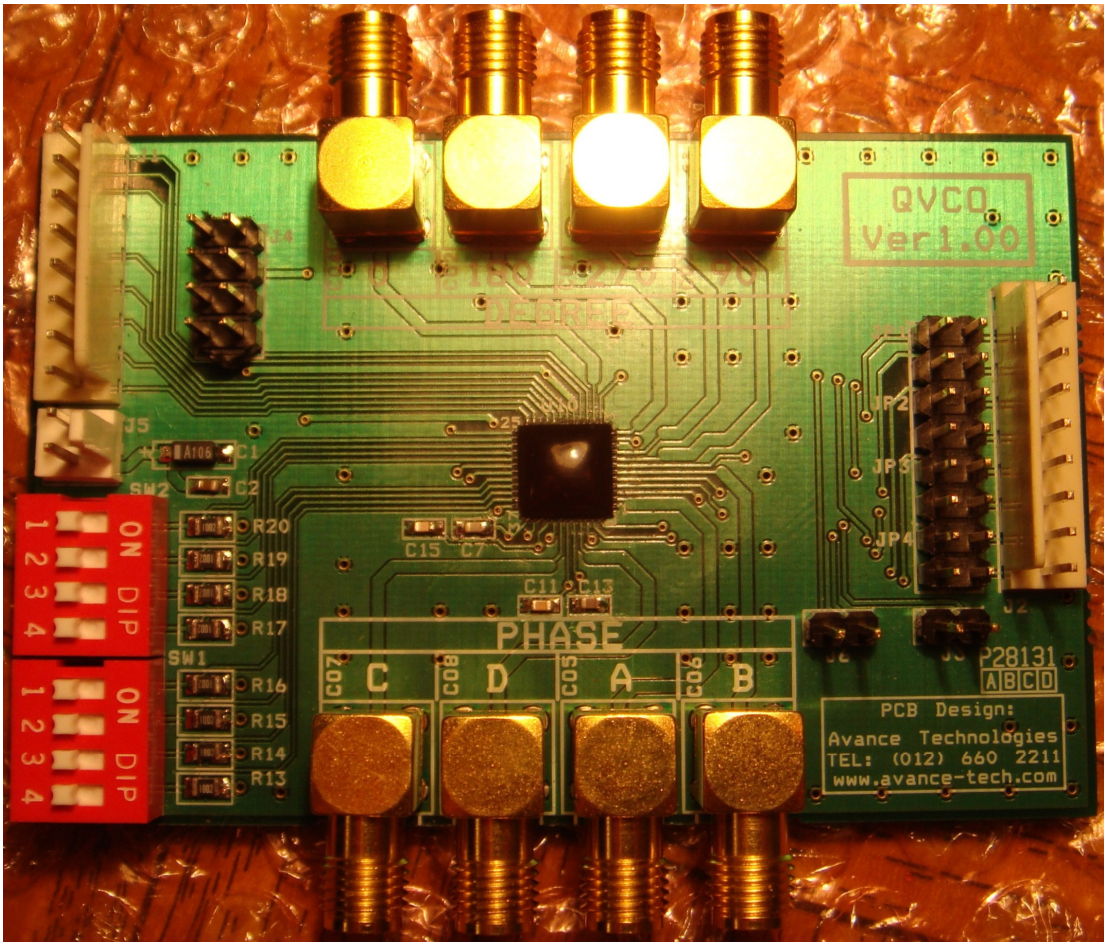


Figure 4.30. A photograph of the PCB design with all the components mounted onto it.

4.13 Conclusion

This chapter explained the design of the core components of the entire circuit, from designing by hand to fine and final optimization through simulations. The chapter started off by characterizing the active and passive components that were to be utilized in the design. This was followed by a detailed design of the quadrature *LC*-VCO, the VGA, the current mirror, the bias circuitry and the digital phase tuner. The way in which these components were integrated in order to realize the final design was then presented and issues related to this integration were then discussed. The floor planning of the IC layout was then shown and the modifications to this initial floorplan to make experimental measurements more practical were then discussed. This was followed by the final IC layout and a chip photograph of the manufactured design. In order to test the IC, an evaluation PCB was designed through a third party company by providing them with a circuit schematic and a list of the desired PCB components. A photograph of this PCB is also shown. The dissertation will now proceed with a presentation of the complete circuit simulation and measurement results.

CHAPTER 5: FULL CIRCUIT SIMULATION AND MEASUREMENT RESULTS

5.1 Introduction

This chapter focuses on the measurement results of this research in order to compare it to the achievements of related work that was reviewed in chapter 2. Chapter 3 presented a discussion on the CAD tools used to simulate this design (section 3.4) and the measurement setup (section 3.5) was also introduced. Chapter 4 showed the IC layout (Figure 4.27) and presented the evaluation PCB used for these measurements (section 4.12). In this chapter the performances of the two core components, namely the quadrature *LC*-VCO and the digital phase tuner is looked at separately. The integration of these components forms the integrated vector sum phase shifter which is the main focus of this research. An evaluation of the phase shifter performance is therefore presented and is then followed by a conclusion which summarizes all the measurement results.

5.2 Quadrature *LC*-VCO

The quadrature *LC*-VCO was simulated with its outputs terminated with the same loads as that of Figure 4.25. Using an *Agilent HP 8563E Spectrum Analyzer* (Agilent Technologies, 2008b) and a *Tektronix DSA72004 Digital Serial Analyzer* (Tektronix Inc., 2008), the quadrature *LC*-VCO (component 2 in Figure 4.27) was measured. The *Agilent HP 8563E Spectrum Analyzer* was last calibrated on 6 June 2008 by *Denel Dynamics* and the *Tektronix DSA72004 Digital Serial Analyzer* was a demo unit from Tektronix that was delivered a week prior to the measurements. Figure 5.1 shows the oscillating frequency as a function of the varactor voltage. The maximum oscillating frequency of the measured oscillator is lower by 11.5 % and the minimum by 9.5 % when compared to the simulation results. This reduction could be attributed towards the parasitic capacitances of the metal in the final circuit layout which lowers the resonating frequency of the tank circuit. The measured frequency tuning range of the oscillator is

$$\text{Tuning range} = \frac{2\left(f_{\max} - f_{\min}\right)}{f_{\max} + f_{\min}} \times 100\,\% = 14\,\%\,. \tag{5.1}$$

Figure 5.2 shows the output power when using a 50 Ω load as a function of the varactor tuning voltage. On average the output power is lower by 9 dB when compared to the

simulation results. This power loss could be attributed to the attenuation of the bond wires, PCB tracks, connectors, coaxial cables and discontinuities in the characteristic impedances.

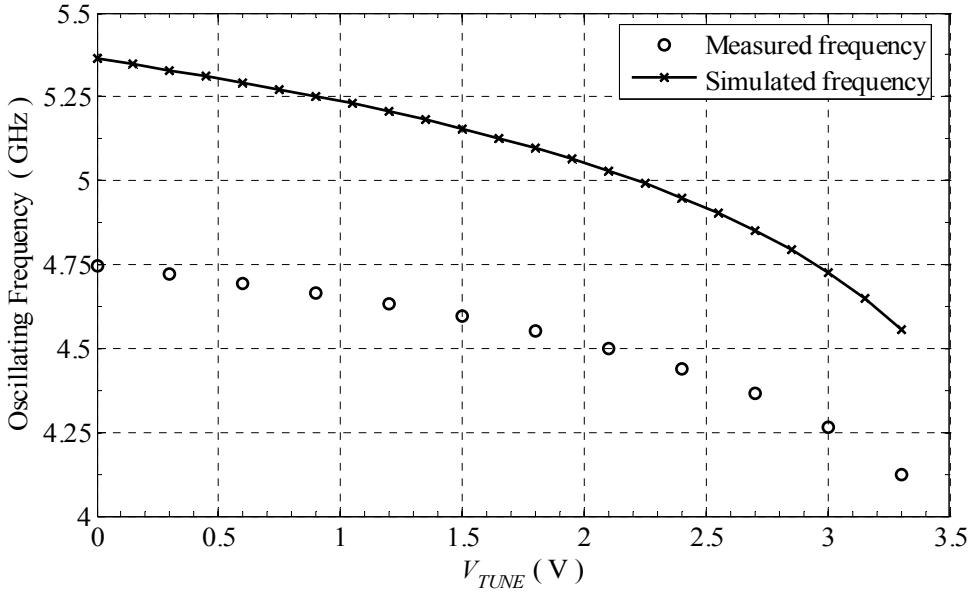


Figure 5.1. Measured and simulated frequency tuning curve of the quadrature *LC*-VCO taken from one of the prototype circuits.

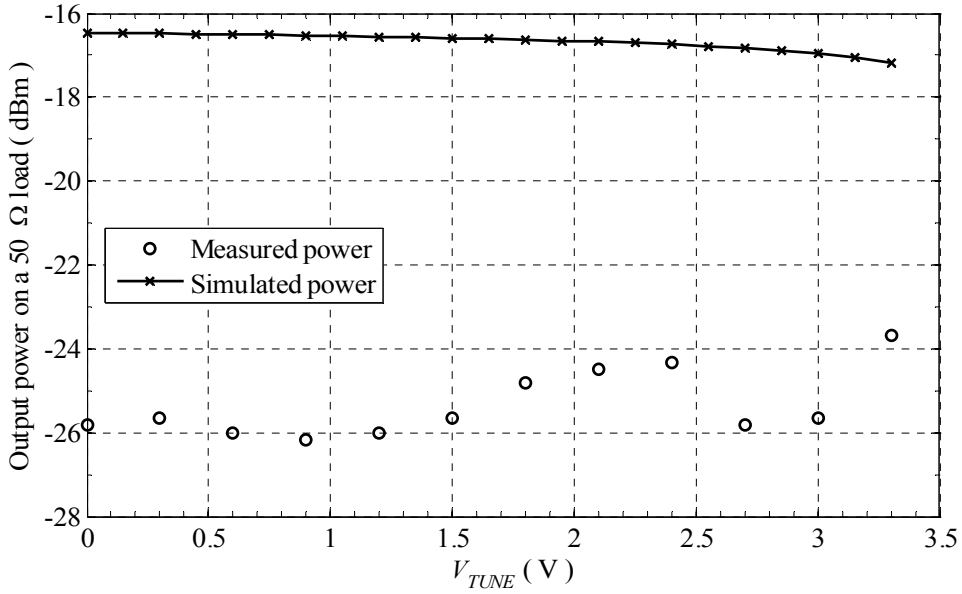


Figure 5.2. Measured and simulated output power when using a 50 Ω load of the quadrature *LC*-VCO over the entire tuning range.

Figure 5.3 shows a screen capture of the phase noise measurements as a function of offset frequency using the *Agilent HP 8563E Spectrum Analyzer*. This specific measurement was done for $V_{TUNE} = 0$ V. More phase noise measurements were done for different values of V_{TUNE} and Figure 5.4 plots and compare these measurements to the simulation results. The FOM of the oscillator for the worst-case phase noise as described in section 2.3 is 157.81 dBc / Hz excluding the output buffer circuitry. The worst case phase noise is found to be -78.50 dBc / Hz at 4.440 GHz at a 100 kHz offset. For a 1 MHz offset, the worst case phase noise is found at 4.124 GHz to be -108.17 dBc / Hz and the FOM for this case is 166.84 dBc / Hz. The oscillator power consumption excluding the buffer circuitry is 23.1 mW.

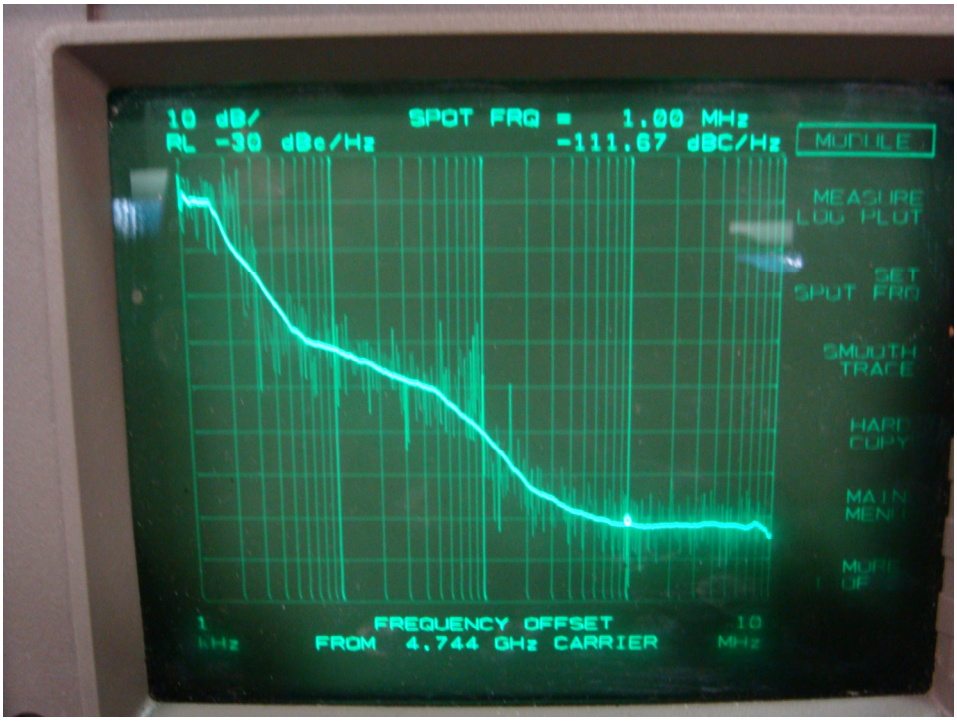


Figure 5.3. A screen capture of the phase noise measurement of the quadrature *LC*-VCO using the *Agilent HP 8563E Spectrum Analyzer*.

Time domain simulations for the quadrature *LC*-VCO were done using the *Tektronix DSA72004 Digital Serial Analyzer* and are shown in Figure 5.5. The maximum sample rate of this oscilloscope is 50 Gs/s and therefore the minimum sampling interval is 20 ps. Even though the sampling rate is well above the Nyquist rate, accurate measurements of the phase difference using fast Fourier transforms (FFT) between the two quadrature signals were not possible because of the poor resolution of the scope at such low voltages as seen from Figure 5.5.

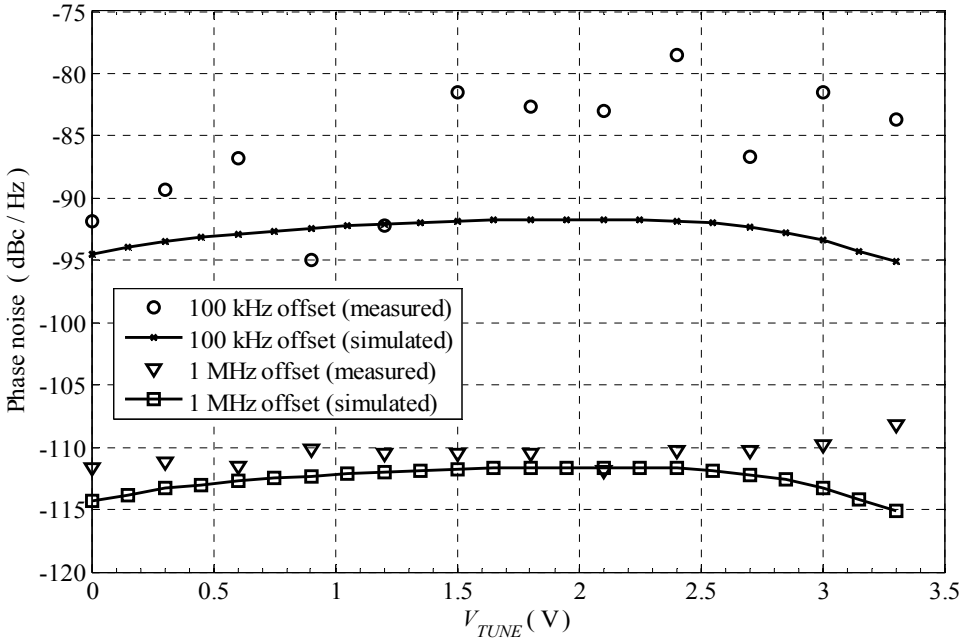


Figure 5.4. The measured and simulated phase noise of the quadrature *LC*-VCO over the entire tuning range

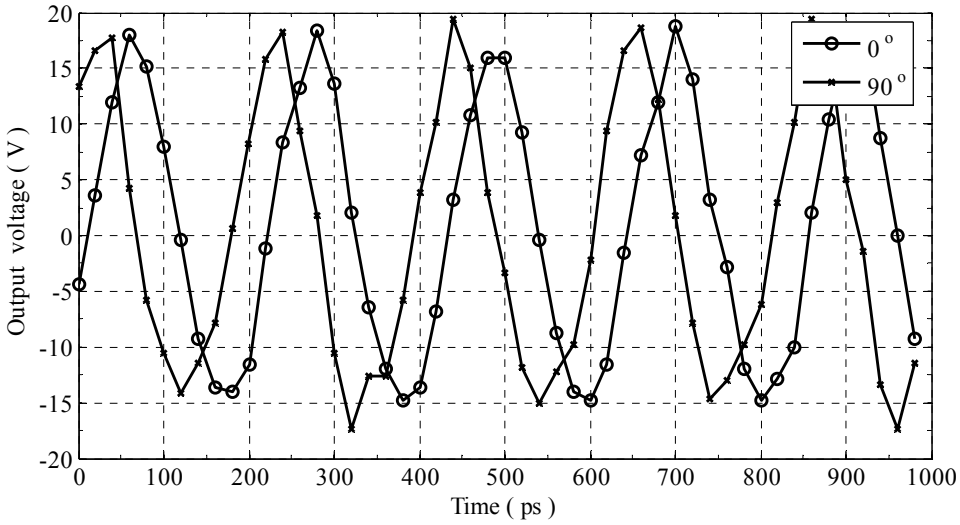


Figure 5.5. A time domain measurement of the quadrature *LC*-VCO for V_{TUNE} = 0 V.

5.3 Digital phase tuner

Outputs V_{1-}, V_{1I+} and V_{1Q+} of the digital phase tuner were measured on pins 1, 7 and 8 respectively, of connector J2 in Figure 4.29. Measurements were done for several different phases using SW2. These measurements were done using a *Fluke 77III Multimeter* (Fluke

Corporation, 2008). The values of ΔV_{1I+} and ΔV_{1Q+} were compared to that of Table VI and the errors are plotted in Figure 5.6.

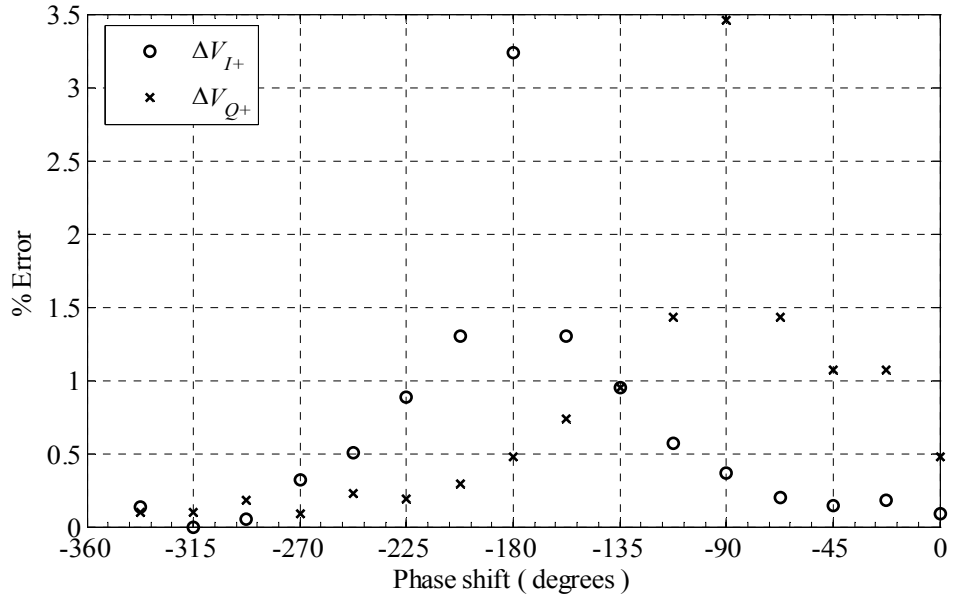


Figure 5.6. Measured errors on the DAC control voltages as compared to Table VI.

The two most significant errors are at -180 ° and -90 ° for ΔV_{I+} and ΔV_{Q+} respectively. At these angles, the values of both V_{I+} and V_{Q+} were supposed to be -0.54 V but were measured to be -0.58 V and -0.59 V respectively. To correct this error, the W / L of M_{25} in Figure 4.22 should be reduced. This error propagated from M_{24} as well since both V_{I+} and V_{Q+} were 20 mV lower than expected at -202.5 ° and -112.5 ° respectively. The W / L of M_{24} in Figure 4.22 should therefore be reduced as well. The output of the modified digital phase tuner, V_{1-} was found to be 1.88 V which is approximately 1.1 % lower than its specification. Since V_{I+}, V_{Q+} and V_{1-} are directly proportional to the W / L of the NMOS transistors, it is recommended that they are scaled in proportion to the measured errors.

5.4 Phase shifter

The output of the phase shifter was measured using the *Agilent HP 8563E Spectrum Analyzer*. The measured output power varies between -52 ~ -42 dBm and the simulated output power between -23 ~ -22 dBm over the entire frequency tuning range. The phase shift was measured using the *Agilent E5071B RF Network Analyzer* for the 16 different DAC presets at 4.72 GHz. Due to limitations in the experimental setup, the tolerances on

the phase measurements are approximately 3 °. The maximum phase error is 35 ° higher than the required phase shift of -135 ° at preset 7. The phase error at -90 ° is only 7 °. This is where the DAC shows the most significant voltage offset.

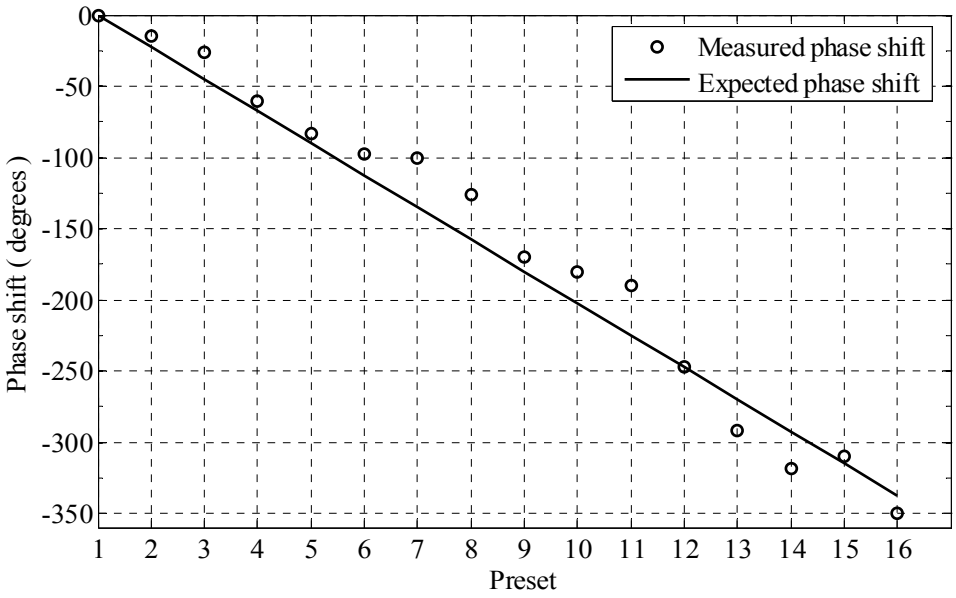


Figure 5.7. Measured phase shift for the 16 different DAC presets along with expected values.

Since Figure 4.21 was used to determine V_{1I+} and V_{1Q+}, any deviation of this simulated graph from its true shape would result in a deviation in amplitude for the in-phase and quadrature currents. The result is a deviation in phase and amplitude. Since the shape of Figure 4.21 was simulated at 5 GHz and is also frequency dependant, it is questionable whether the values obtained for V_{1I+} and V_{1Q+} are optimal. This prediction is supported by Figure 5.8 which plots this simulated transfer curve at various frequencies. To correct these phase errors, the V_{1I+} and V_{1Q+} values at the different presets should be determined based on the transfer curves in Figure 5.8 at the closest frequency. The modular IC layout allows the V_{1I+} and V_{1Q+} inputs of component 1 in Figure 4.27 to be controlled externally.

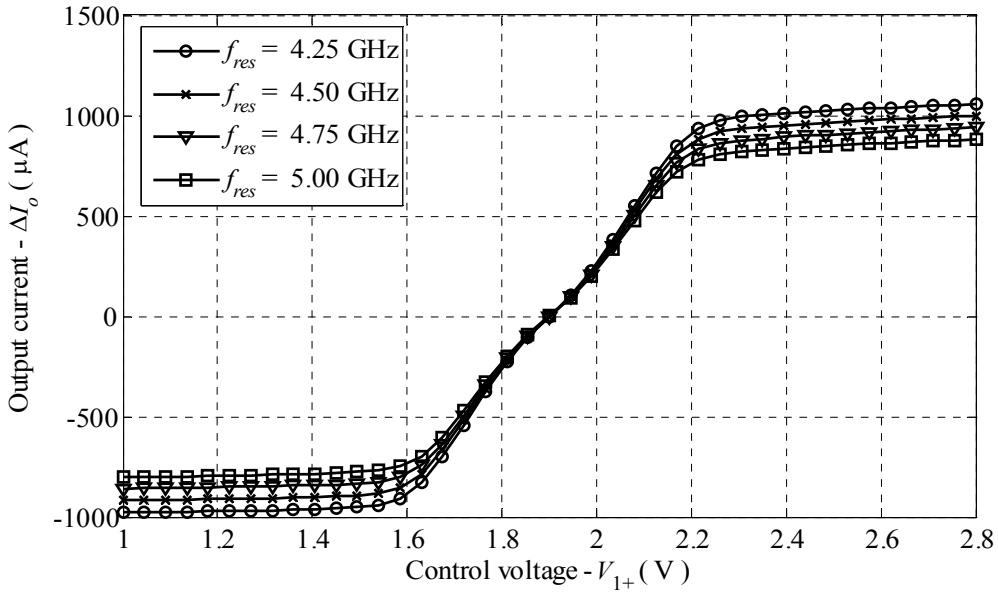


Figure 5.8. The simulated voltage-to-current transfer function of the VGA at various frequencies.

5.5 Conclusion

The chapter described the measurement results of the manufactured circuit and compared it to the simulation results. These measurement results shows that the quadrature *LC*-VCO oscillates on average 10.5 % slower and delivers 9 dB less power to the spectrum analyzer when compared to the simulations results. It was found that the output voltages of the DAC are within 3.5 % of the design specifications. Phase shift measurements shows that the phase errors are as large as 35 ° and this could be attributed to the frequency dependence of the voltage-to-current transfer curve of the mixer as supported by simulation results. The dissertation will now conclude in the following chapter by summarizing this work and making some suggestions for future work.

CHAPTER 6: CONCLUSION

6.1 Introduction

Chapter 2 discussed relevant research outputs of previous designs from literature. This chapter aims to summarise the contributions of this research. The summary is developed based on the circuit designs of chapter 4 and the measurement results of chapter 5. Suggestions for future work are also mentioned and conclude this chapter.

6.2 Technical summary and contribution

This main contribution of this research involves the design and measurement of a SiGe BiCMOS vector sum phase shifter at 5 GHz to be implemented at the LO used for RF up or down conversion. Measurement results not only prove that this concept can be realised, but also suggest enhancements to this design to make its implementation more practical.

The following lists the technical specifications of the entire design:

- Process: AMS 0.35 µm SiGe BiCMOS
- Supply voltage: 3.3 V
- VCO architecture: quadrature *LC*
- VCO frequency range: 4.12 ~ 4.74 GHz
- Maximum phase noise (at 100 kHz offset): -78.50 dBc / Hz
- Maximum phase noise (at 1 MHz offset): -108.17 dBc / Hz
- VCO power consumption (excluding buffer circuitry): 23.1 mW
- VCO FOM: 157.81 dBc / Hz
- Number of phase shifters: 4
- Phase shifter tuning range: 360 °
- Phase shifter resolution: 22.5 °
- Phase shifter accuracy: < 10 %
- Power consumption per phase shifter: 62.2 mW
- Total power consumption: 281.1 mW
- Chip area - I/Q VCO with 4 × 360 ° phase shifters: 1.10 × 0.85 mm^2.
- Chip area - digital phase tuner: 0.41 × 0.13 mm^2.

6.3 Recommendations for future work

Quadrature *LC*-VCO measurements show that the oscillating frequency is on average 10.5 % lower than was predicted by circuit simulations. This error is most likely introduced by parasitic impedances introduced by the metals used in the circuit layout. In future, special effort must be made to extract these impedances from the circuit layout using CAD tools and include them into the final circuit simulations. Additionally the layout can be done using a practical layout method called Ground Shield Microstrip Lines (GSML) (Lee *et al*., 2007). Using this method a ground shield is inserted below the connecting metal nodes of the layout and the parasitic impedances can be modelled using TLs.

The measured phase noise of the quadrature *LC*-VCO is comparable to that obtained in literature for similar designs. As discussed in section 4.5, the differential inductor used was selected from a list of available inductors which were designed and measured by the IC foundry. In order to improve the phase noise performance of the circuit, a custom differential inductor could be designed that delivers its peak performance at the frequency of interest (Božanić and Sinha, 2007).

The measured output power for the VCO is on average 9 dB lower than was predicted by simulation results and 25 dB lower for the entire phase shifter. The origin of this error could arise from two sources. Firstly, the simulated output impedance of both devices could be different from the physical output impedance after layout due to parasitic impedances introduce by the metals. This would increase the load mismatches and result in a significant power loss. Secondly the power loss could be attributed to the attenuation of the bond wires, PCB tracks, connectors, coaxial cables and discontinuities in the characteristics impedances as mentioned in section 5.2. This second source of power loss is of no real concern to this design since it is to be integrated on chip with various other communication circuits. For measurement purposes however, it was found that the low signal power from the entire phase shifter made accurate phase noise and phase difference measurements difficult because the signal is close to the noise floor of the equipment. It is recommended that power output stages are designed to allow for more accurate and reliable measurements. While measurements were done it was also found that the spacing

between the SMA connectors of the PCB in Figure 4.30 was too narrow. At times it was inconvenient to find cables that would fit next to each other because of this narrow space.

As was mentioned in section 4.8 the bias circuitry was not designed to be insensitive to power supply and temperature deviations. A full implementation of this circuit would require these components to be designed to be less sensitive to these variations according to some design specifications.

Phase errors from the phase shifter that are as large as 10 % would in most cases be unsuitable for a practical implementation. Even though great care was taken to ensure that the phase errors at 5.0 GHz were as low as possible, the performance at 4.7 GHz does not reflect this. It shows the difficulty involved in designing accurate phase shifting over a wide variety of circuit parameters. In future, it is suggested that the control signals to the phase shifter are adjusted using feedback from circuitry that measures the current phase difference. For example, a negative phase error means that V_{Q+} should be increased whilst V_{I-} is reduced and vice versa for a positive phase error. A similar approach could also be taken to ensure that a constant amplitude over the entire tuning range is maintained. Such a proposed design would make the phase shift less sensitive to parameter variations. Because the control signals from the digital phase tuner are not internally connected to the phase shifter, it would be possible to test this concept on this design using separate external circuitry.

The cost of a full CMOS implementation should be investigated to determine if this solution would meet performance requirements at a reduced price. The decision to use SiGe BiCMOS technology was motivated by the superior high frequency performance of this technology when compared to others from the same manufacturer, as discussed in section 1.5. A lower cost implementation of the design with an acceptable performance as required by its application would make it more attractive for commercialisation.

The design specifications developed were not based on the requirements set by a specific application. For example, the design could be adapted to meet the requirements set by the proposed 802.11n draft (IEEE P802.11 - Task Group N, 2008). Trade-offs such as phase noise, power consumption and circuit area should be considered carefully for such an application.

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APPENDIX A: DIGITAL DECODER – VHDL CODE AND CIRCUIT SCHEMATIC

The following shows the complete VHDL code that was used in order to design the digital decoder discussed in section 4.9. The circuit schematic of the digital decoder is also shown and its layout follows in Appendix B.

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;

ENTITY phaseshift IS
PORT
(phaseSel: in std_logic_vector(3 downto 0);
IPhase: out std_logic_vector(7 downto 0);
Qphase: out std_logic_vector(7 downto 0));
END phaseshift;

ARCHITECTURE arch OF phaseshift IS
BEGIN
mapping: Process(phaseSel)
Begin
case phaseSel is
when "0000" =>
IPhase<= "11111111";
Qphase<= "00001111";
when "0001" =>
IPhase<= "01111111";
Qphase<= "00011111";
when "0010" =>
IPhase<= "00111111";
Qphase<= "00111111";
when "0011" =>
IPhase<= "00011111";
Qphase<= "01111111";
when "0100" =>
IPhase<= "00001111";
Qphase<= "11111111";
when "0101" =>
IPhase<= "00000111";
Qphase<= "01111111";
when "0110" =>
IPhase<= "00000011";
Qphase<= "00111111";
when "0111" =>
IPhase<= "00000001";
Qphase<= "00011111";
when "1000" =>
```

```
IPhase<= "00000000";
Qphase<= "00001111";
when "1001" =>
IPhase<= "00000001";
Qphase<= "00000111";
when "1010" =>
IPhase<= "00000011";
Qphase<= "00000011";
when "1011" =>
IPhase<= "00000111";
Qphase<= "00000001";
when "1100" =>
IPhase<= "00001111";
Qphase<= "00000000";
when "1101" =>
IPhase<= "00011111";
Qphase<= "00000001";
when "1110" =>
IPhase<= "00111111";
Qphase<= "00000011";
when "1111" =>
IPhase<= "01111111";
Qphase<= "00000111";
when others =>
IPhase<= "11111111";
Qphase<= "11111111";
end case;
end Process;
END arch;
```

Figure A.1. VHDL code used to design the digital decoder.

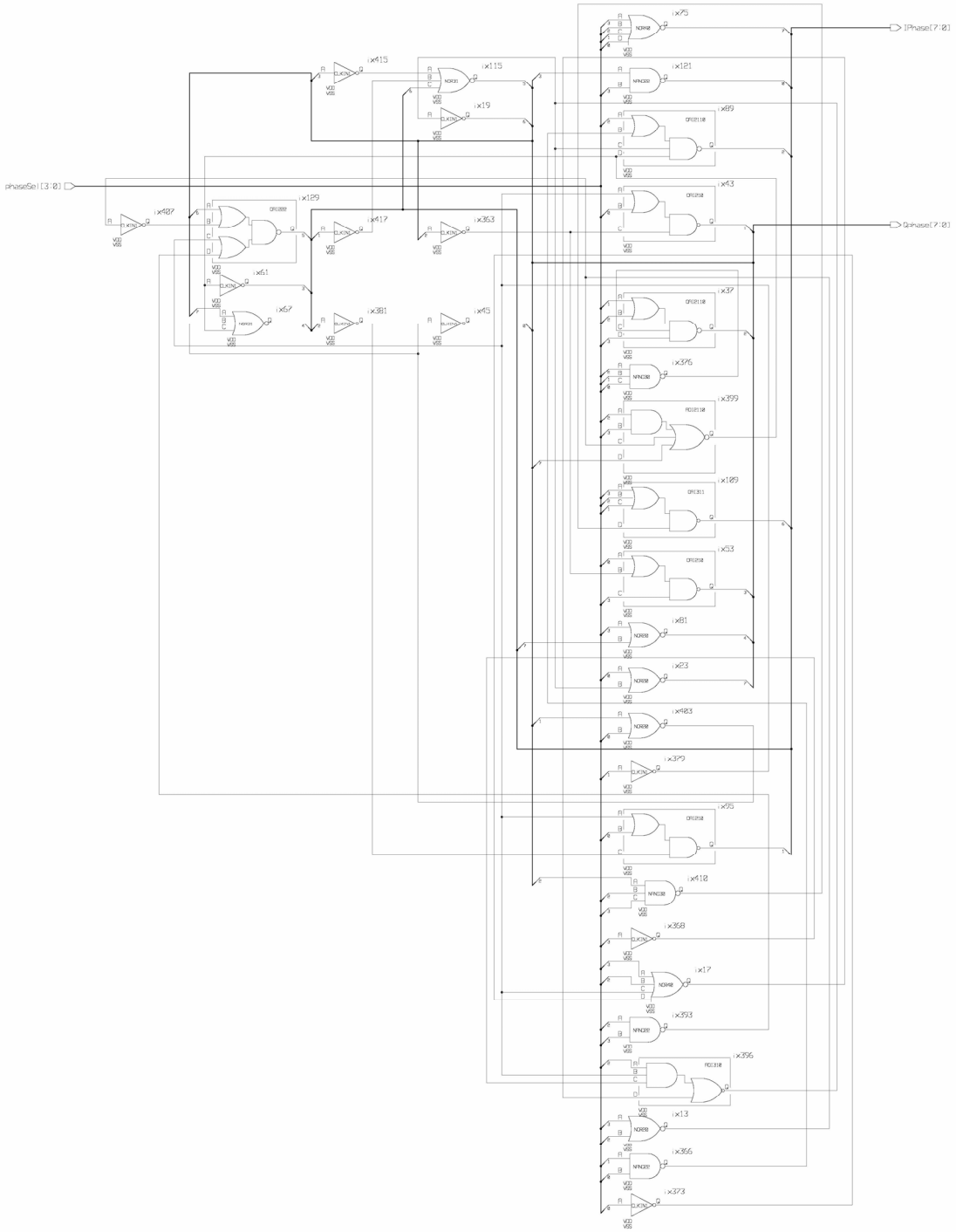

Figure A.2. Circuit schematic of the digital decoder that was generated using the VHDL code of Figure A.1.

APPENDIX B: DETAILED CIRCUIT LAYOUTS

The following shows more detailed figures of the main layouts as discussed in section 4.11. In particular, components labelled 1-6 in Figure 4.27 are shown in Figure B.2-Figure B.7 respectively with more detail. The legend of the layout is shown in Figure B.1 and the layout of the digital decoder is shown in Figure B.8. The bonding diagram of the QFN package is shown in Figure B.9. Chip photographs of components labelled 1,2,4 and 5 in Figure 4.27 are shown in Figure B.10-Figure B.13 respectively.

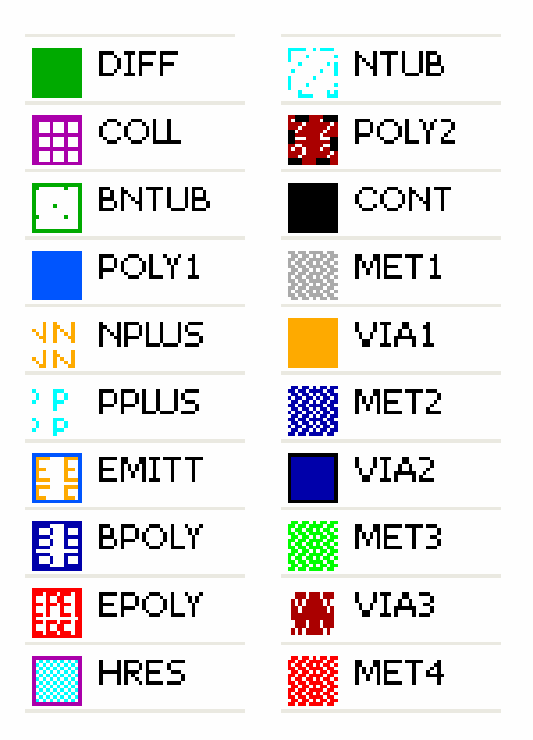

Figure B.1. Legend of the layouts that follow.

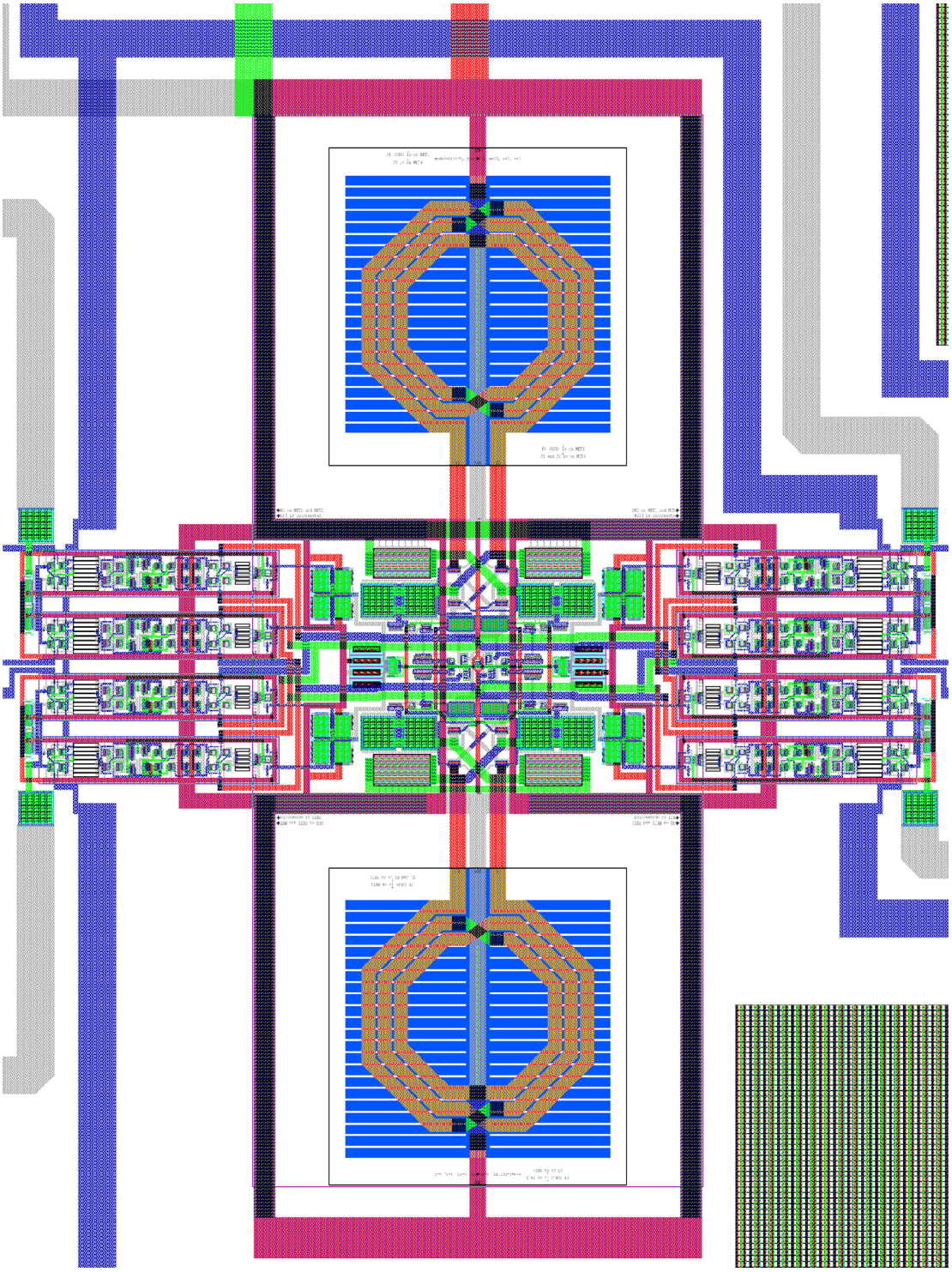

Figure B.2. Layout of the complete circuit, excluding the digital phase tuner.

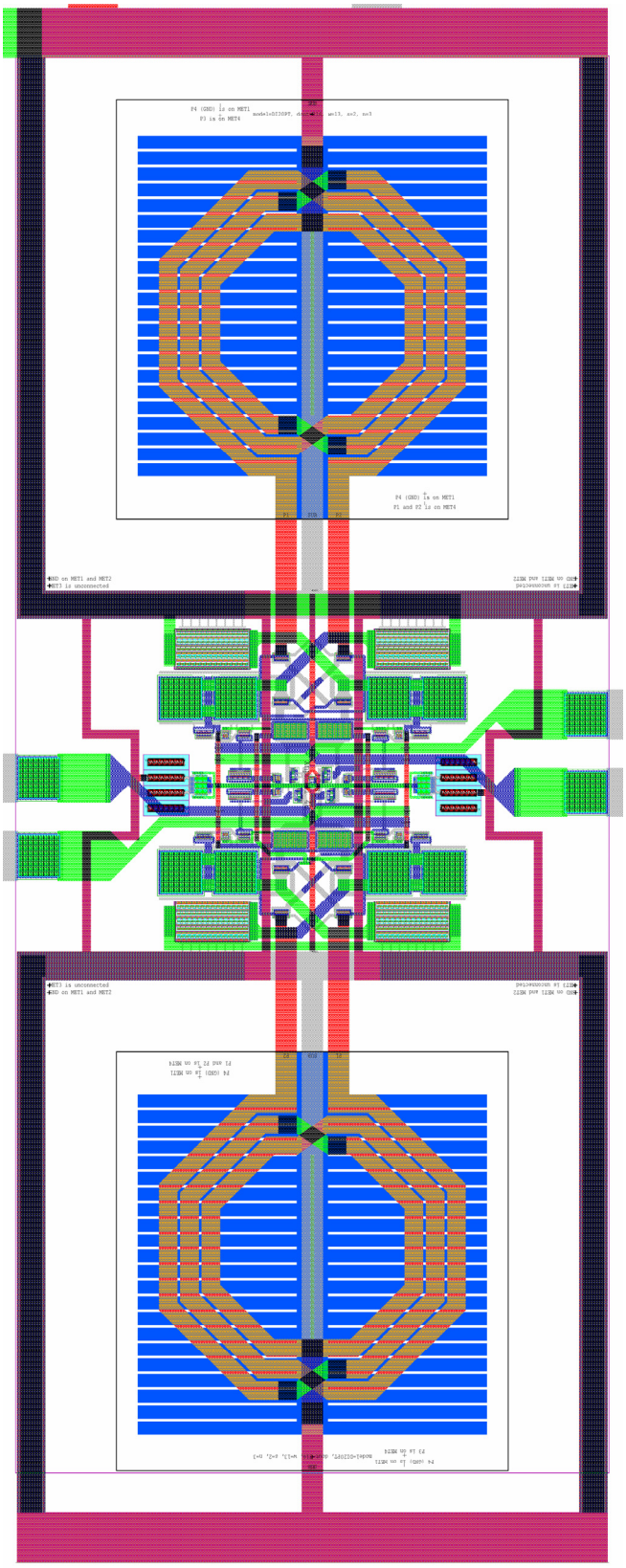

Figure B.3. Quadrature *LC*-VCO layout.

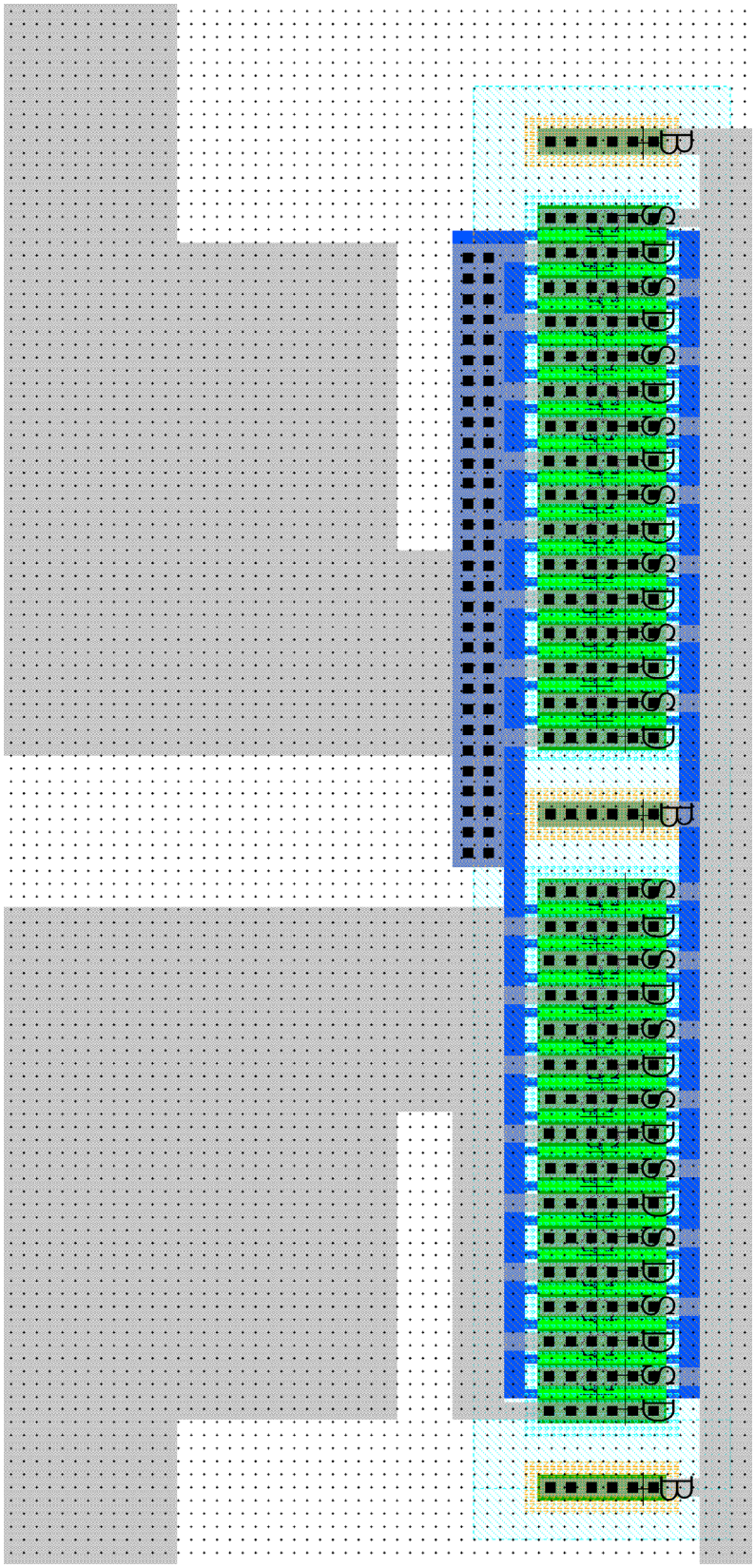

Figure B.4. Single current mirror layout.

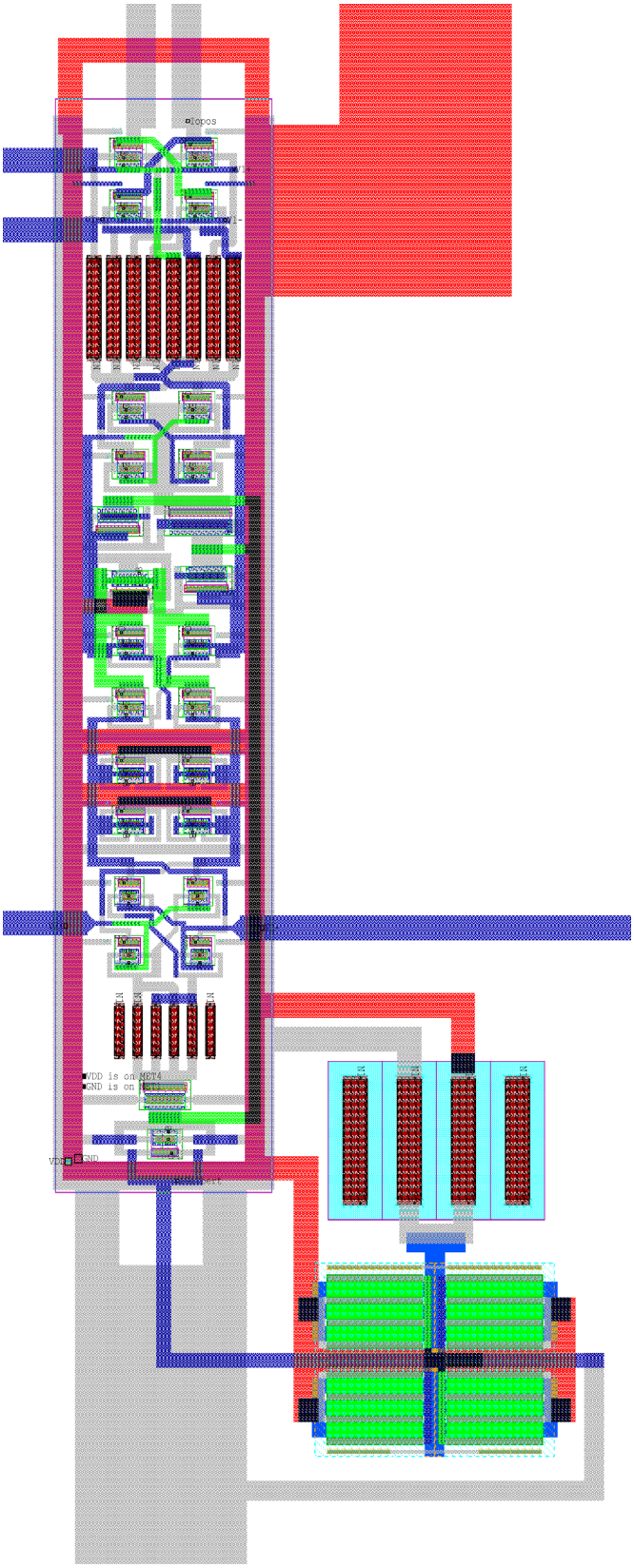

Figure B.5. VGA biased using an 800 µA current source.

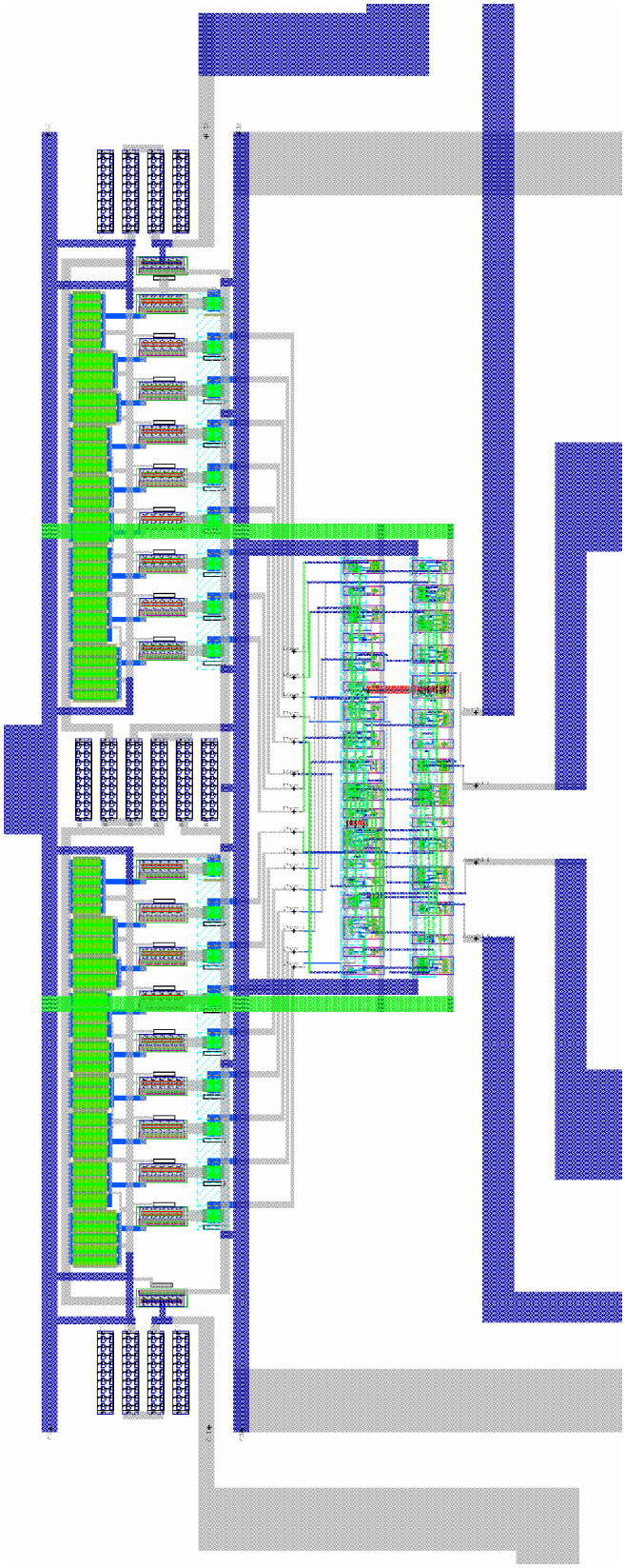

Figure B.6. Complete digital phase tuner.

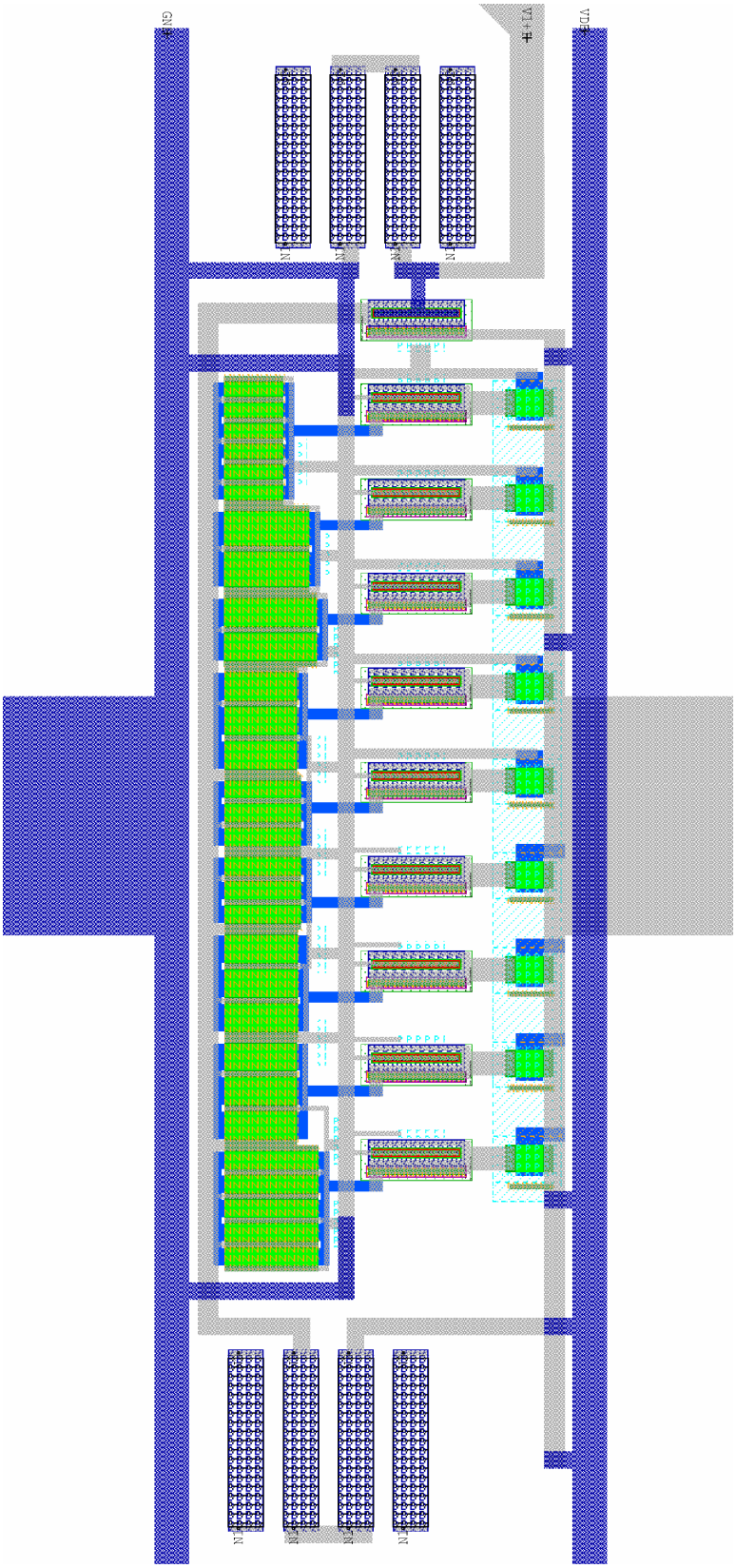

Figure B.7. Modified digital phase tuner.

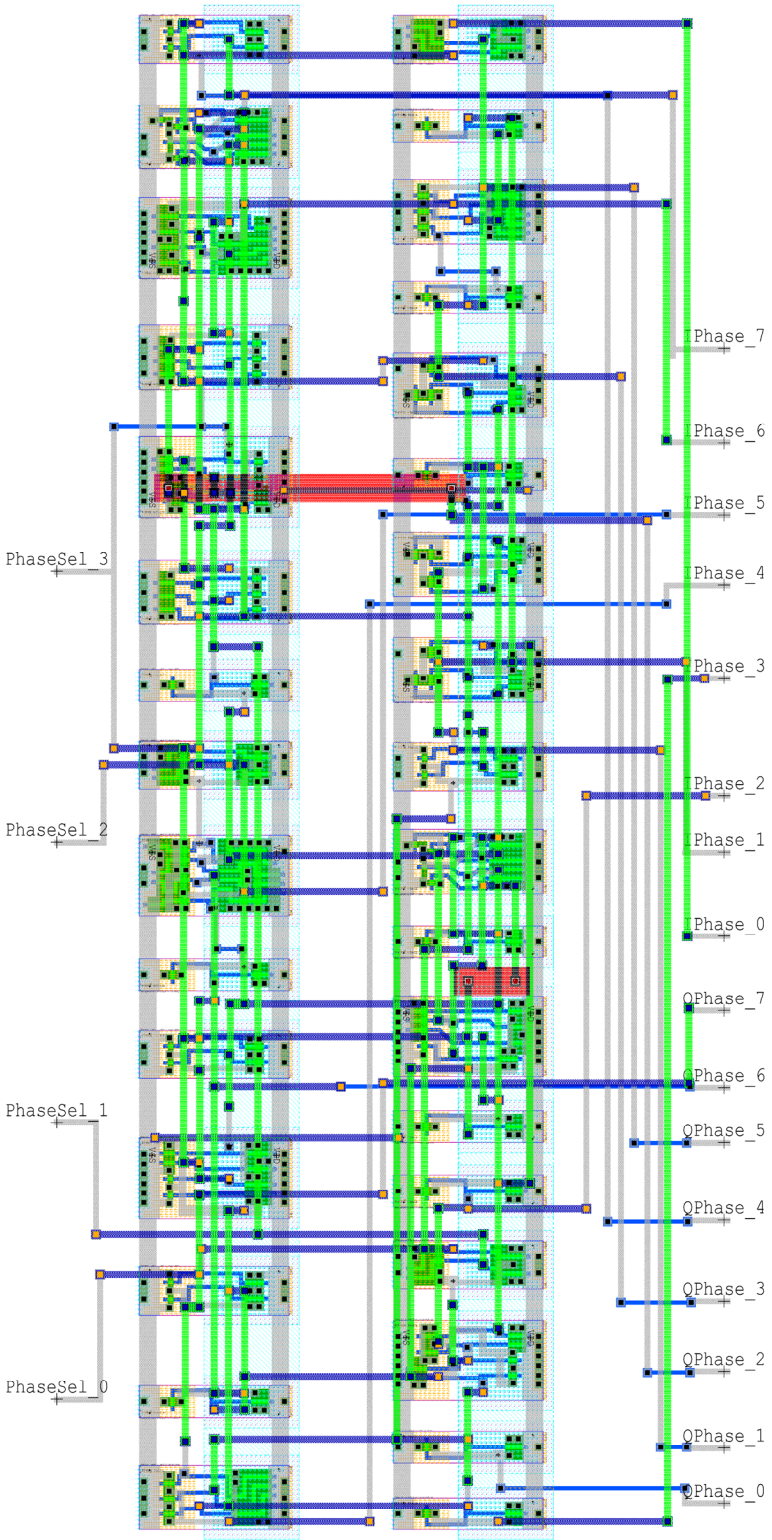

Figure B.8. Detailed layout of the digital decoder. The layout was automated from VHDL code using the Mentor Graphics® package and corresponds to the circuit schematic in Figure A.2.

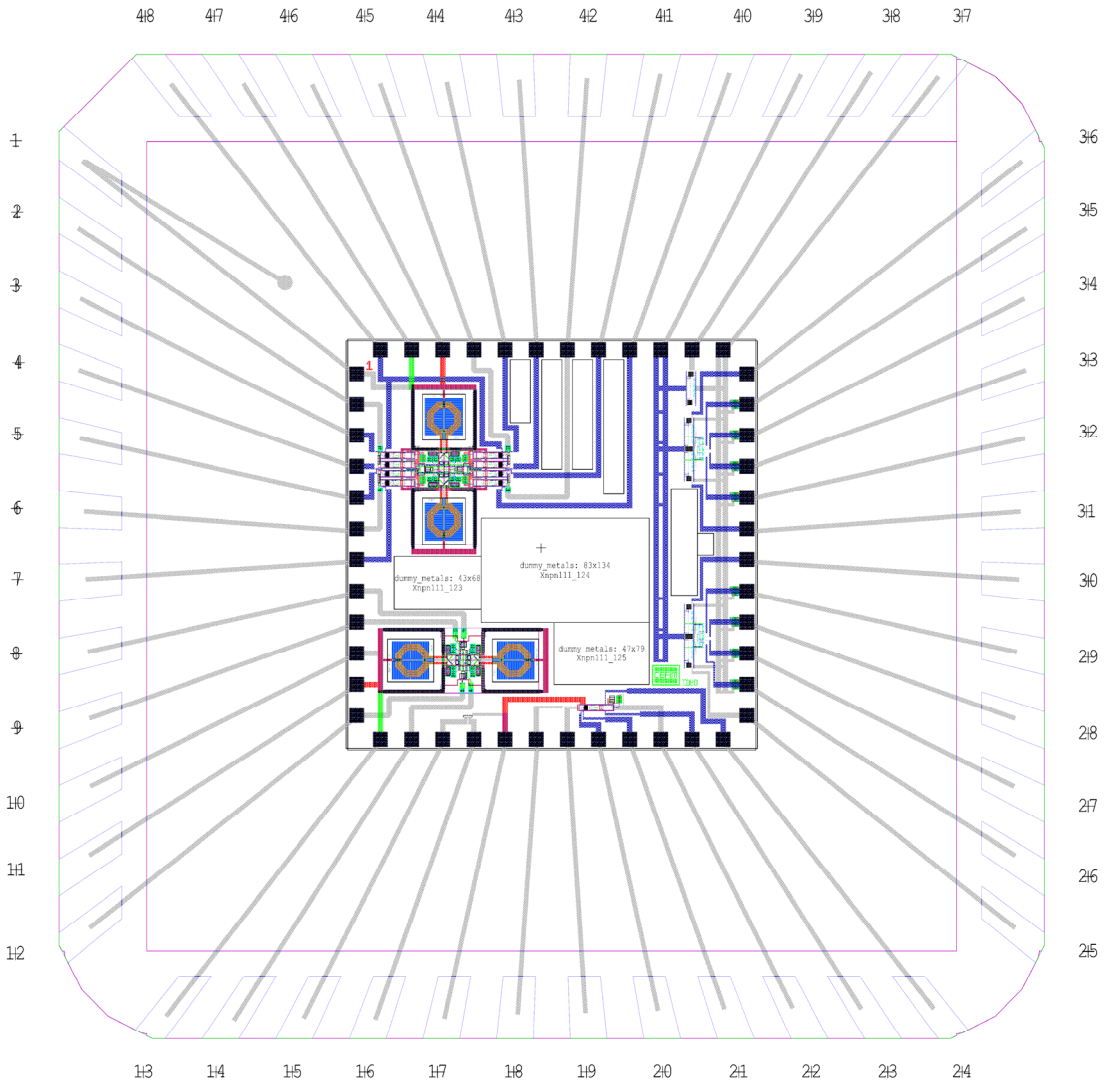

Figure B.9. Bonding diagram of the QFN 48 package.

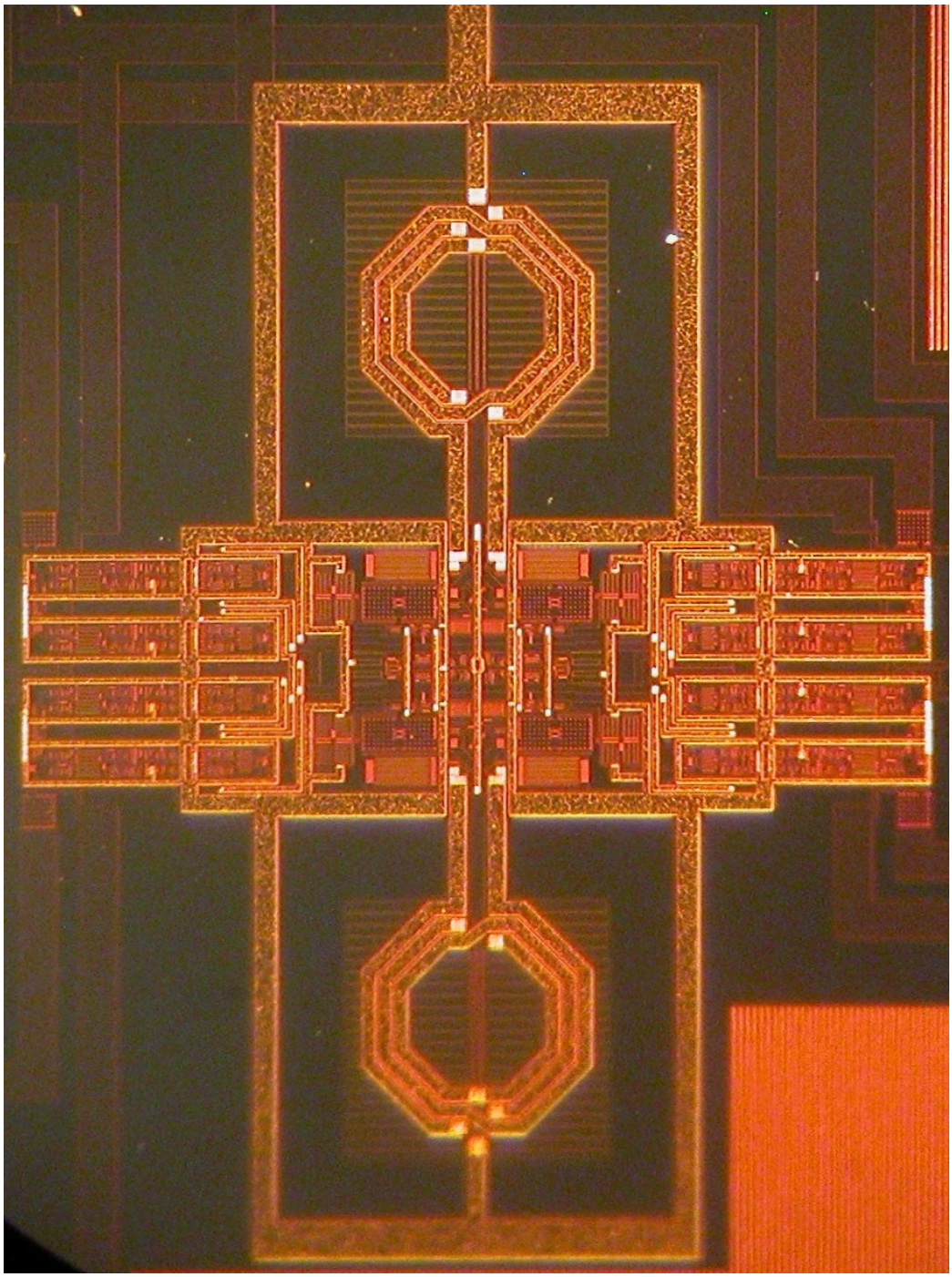

Figure B.10. Photograph of the complete circuit, excluding the digital phase tuner.

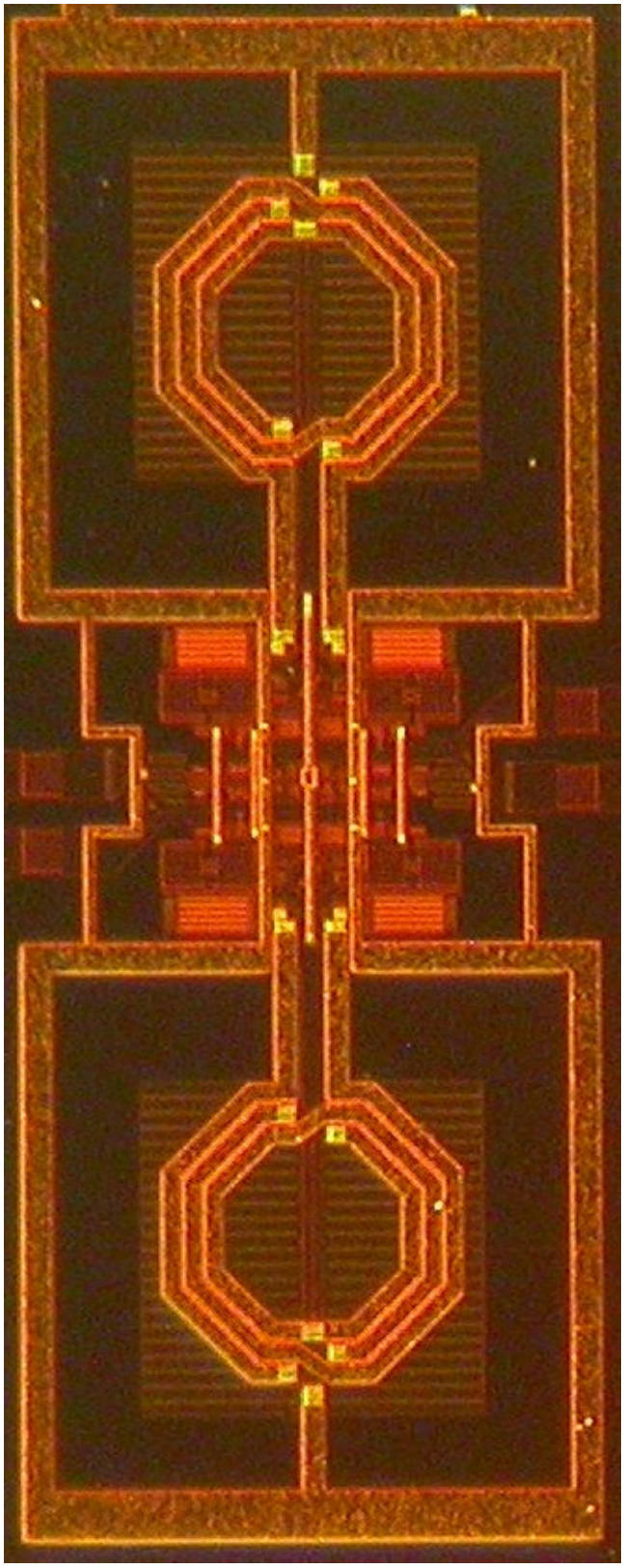

Figure B.11. Quadrature *LC*-VCO photograph.

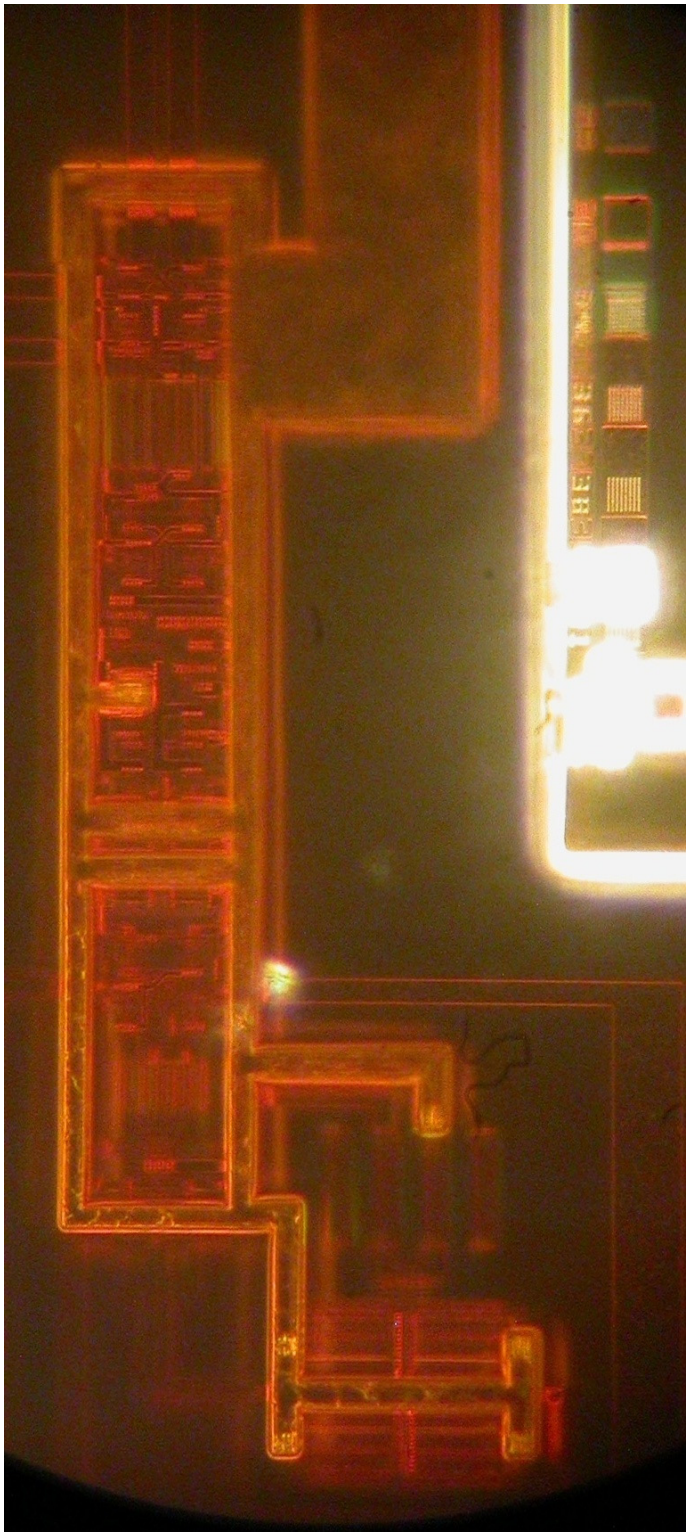

Figure B.12. Photograph of the VGA biased using an 800 µA current source.

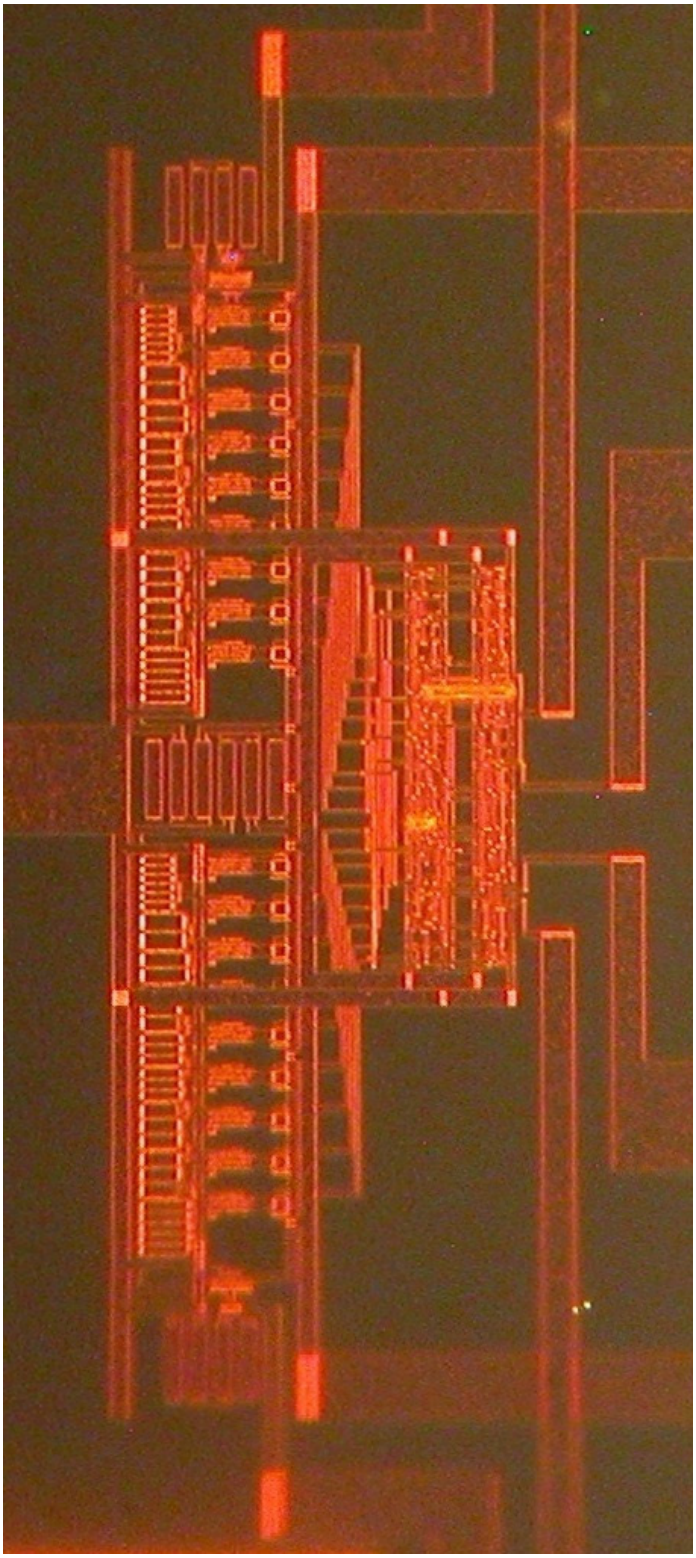

Figure B.13. Photograph of the complete digital phase tuner.